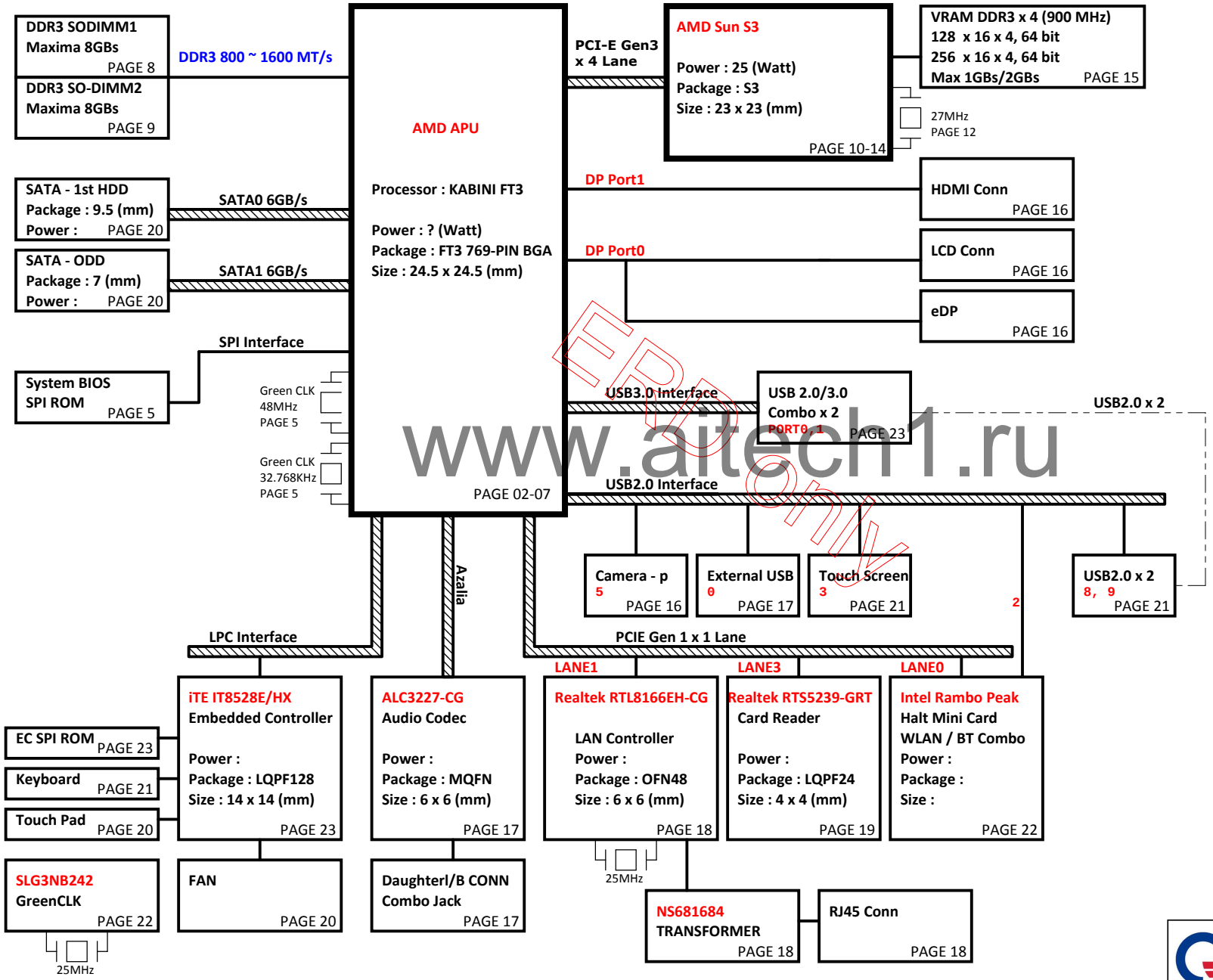
Lean G_AMD KABINI DIS/UMA (14"/15.6") Ultra/Slim 01



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SVCC
LAYER 6 : BOT

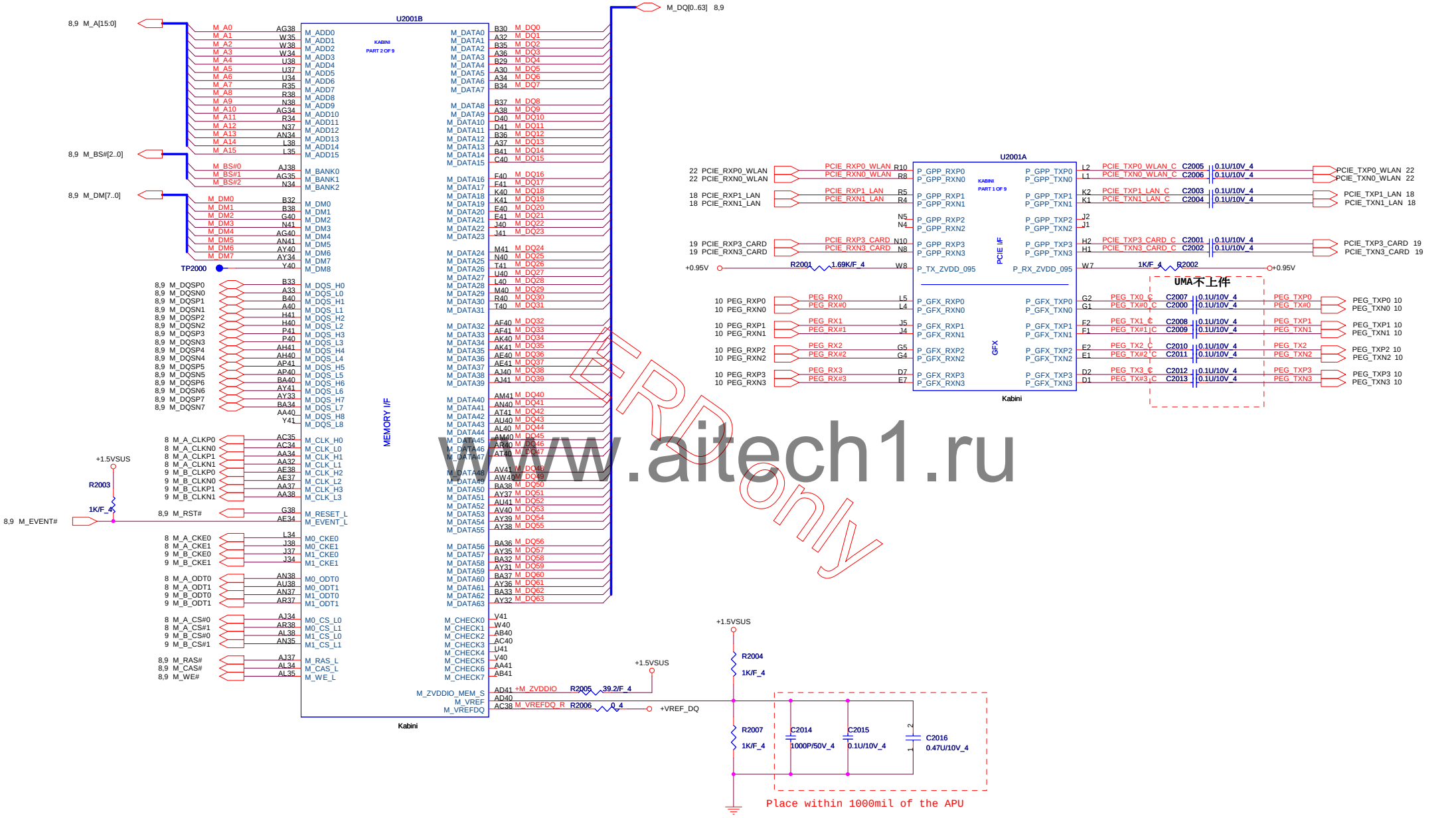
Power Source

- TI BQ24728 — System Charge Power (+BATCHG) — PAGE 24
- Ricktek RT8223PZ — System Power (+3VPCU/+5VPCU/+3VS5/+5VS5) — PAGE 25
- AOZ1237QI/APW8824CTI/G9183 — KABINI Power (+0.95V/+0.95VS5/+1.5VS5) — PAGE 26
- TI TPS51216 — System Memory Power (+1.5VSUS/+0.75V_DDR_VTT)
  Richtek RT8068A — KABINI Power (+1.8VS5) — PAGE 27
- Intersil ISL6277HRTZ/ISL6208BCRZ — Processor Power (+VCC_CORE/+VDDNB_CORE) — PAGE 28~29
- GMT G5934RZ1U — System Discharge Power (+1.5V/+3V/+5V)(+3VSUS/+3VLANVCC/+1.8V) — PAGE 30
- On-semi ADP3211A — VGA Power (+VGA_CORE) — PAGE 31
- Richtek RT8086A — DGPU Power (+1.0V_VGA/+3V_VGA/+1.5V_VGA/+1.8V_VGA/) — PAGE 32

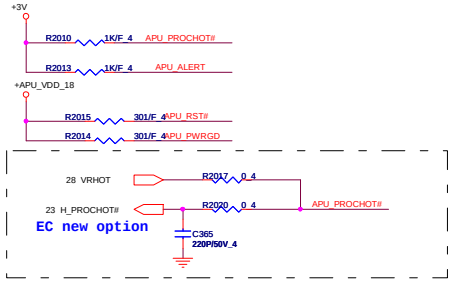
PROJECT :U93
Quanta Computer Inc.

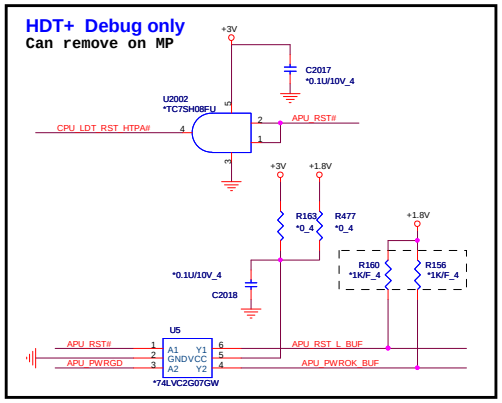
Size	Document Number	Rev
A3	Block Diagram	1A

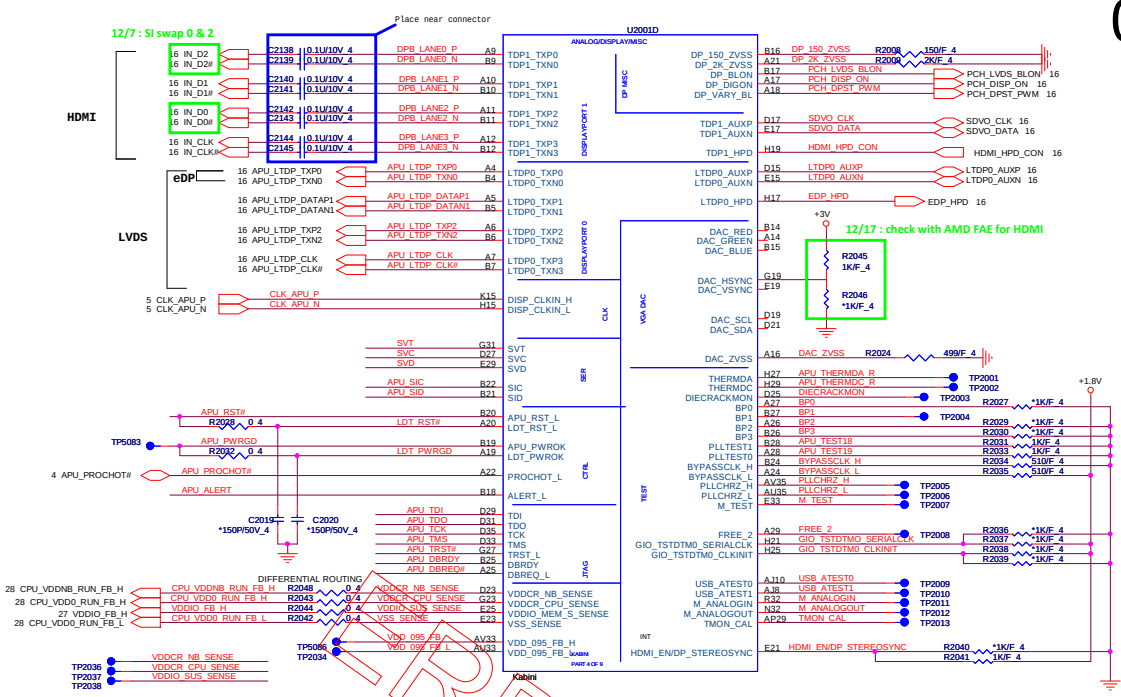
Date: Wednesday, April 03, 2013 Sheet 1 of 32



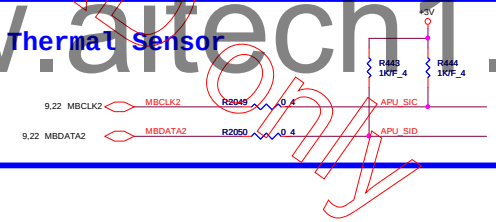
INT	PROJECT :U93 Quanta Computer Inc.		
Size	Document Number MEM/PCIE (1/6)	Rev 1A	
Date: Wednesday, April 03, 2013	Sheet 2 of 32		



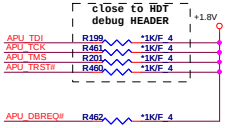


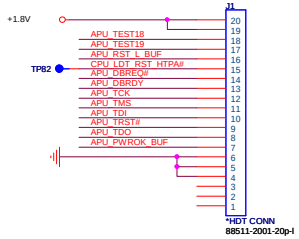


Thermal Sensor

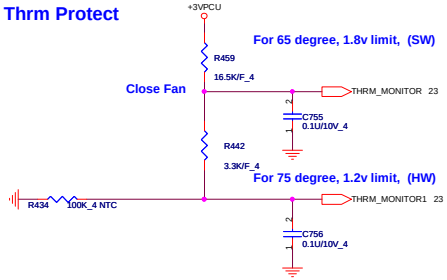


HDT+ Connector for Debug only

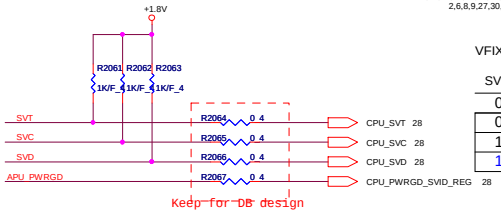


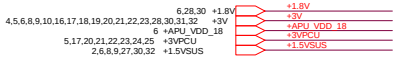


IO Thrm Protect



Serial VID



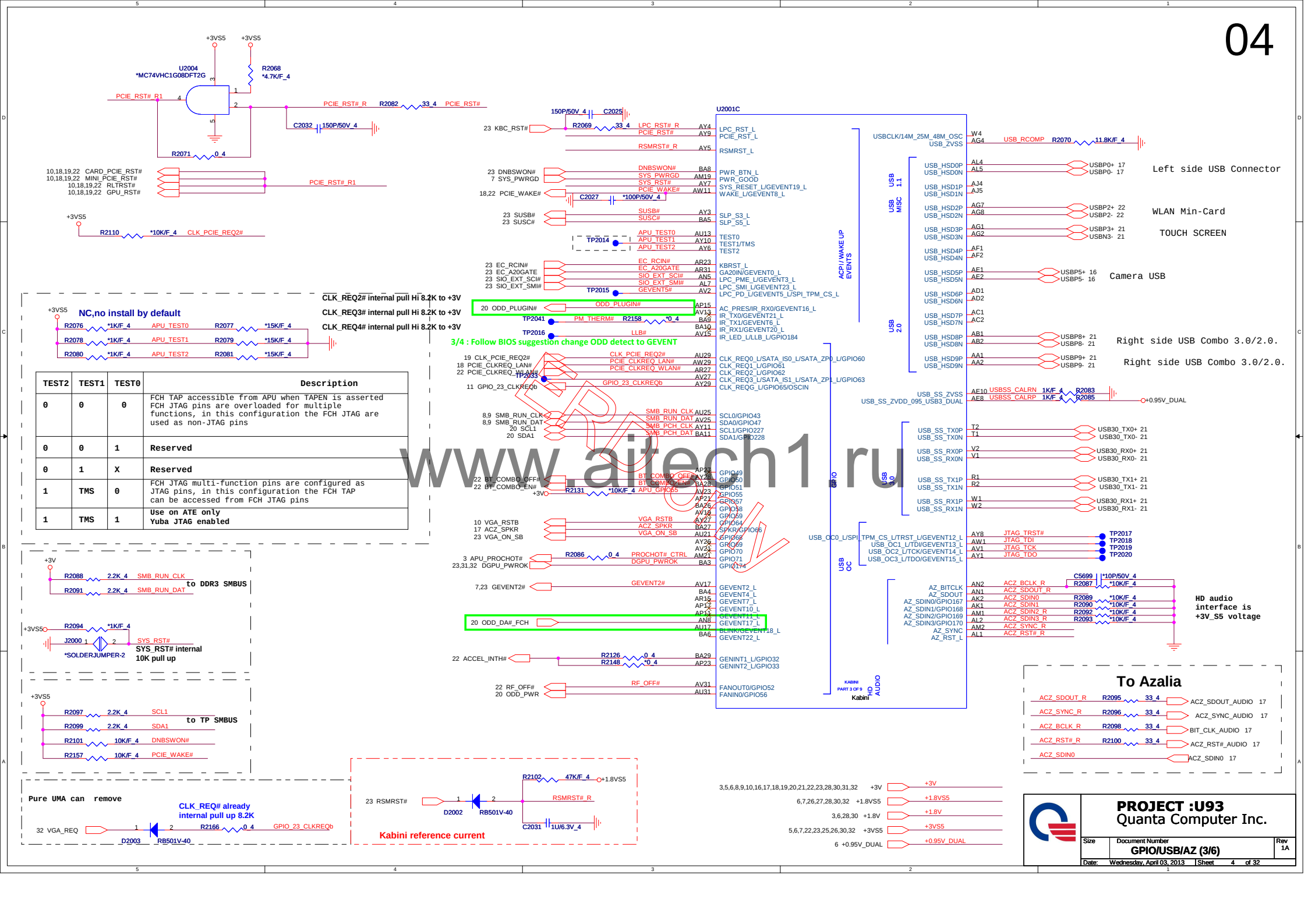


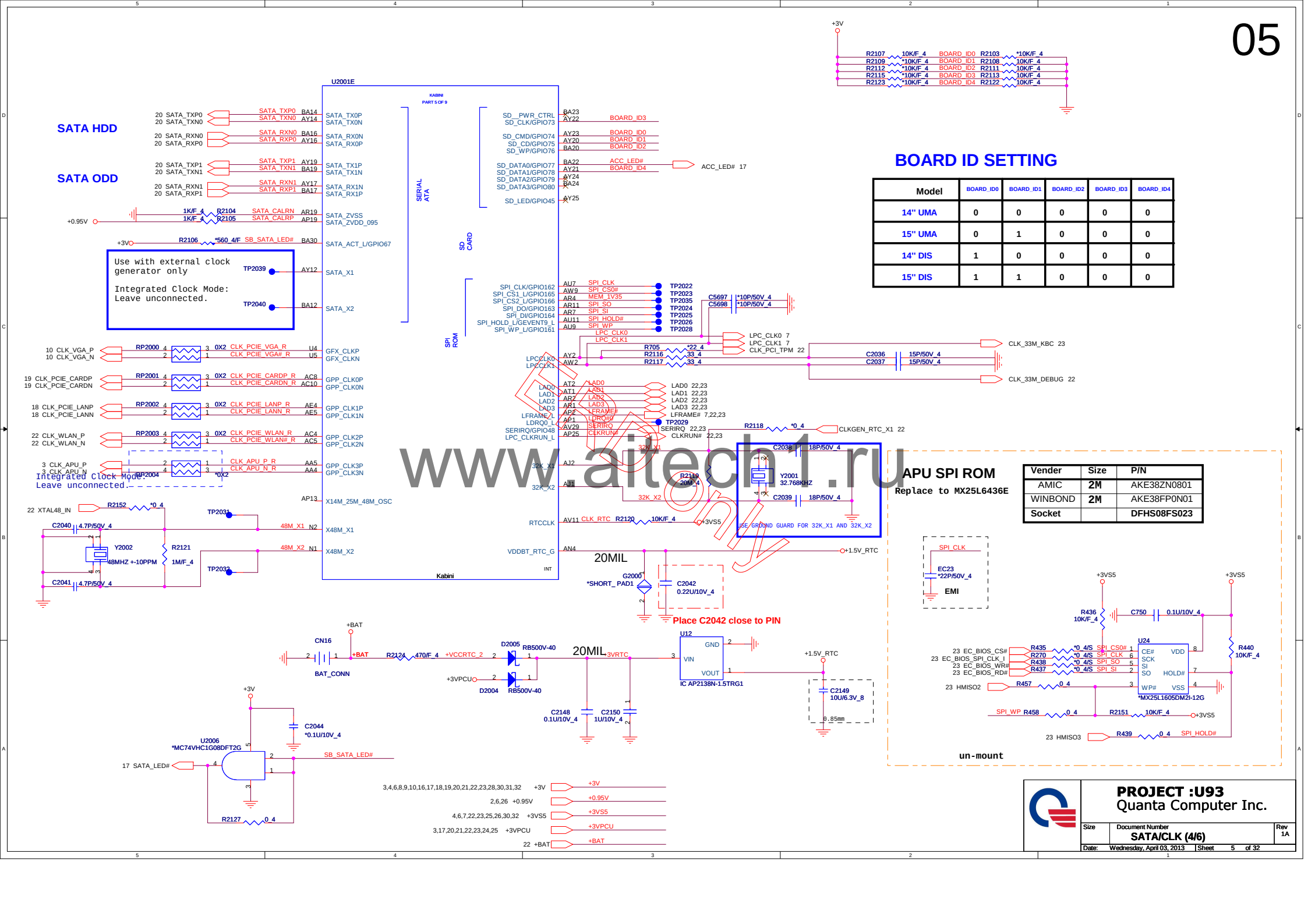
VFIX MODE — VID Override table (VDD)

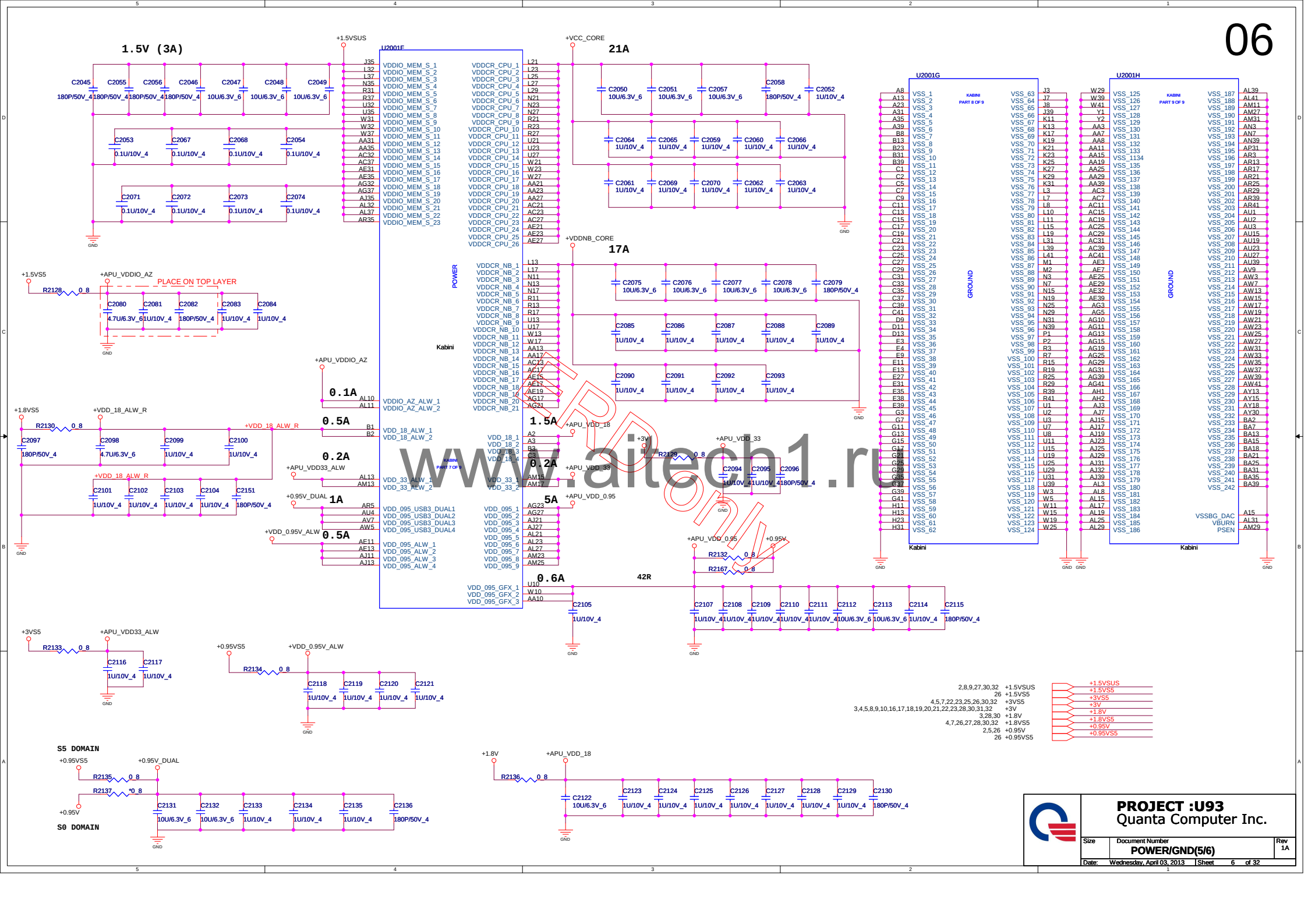
SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

PROJECT :U93
Quanta Computer Inc.

Size	Document Number	Rev
	DIS/MI (2/6)	1A
Date: Wednesday, April 03, 2013	Sheet 3 of 32	

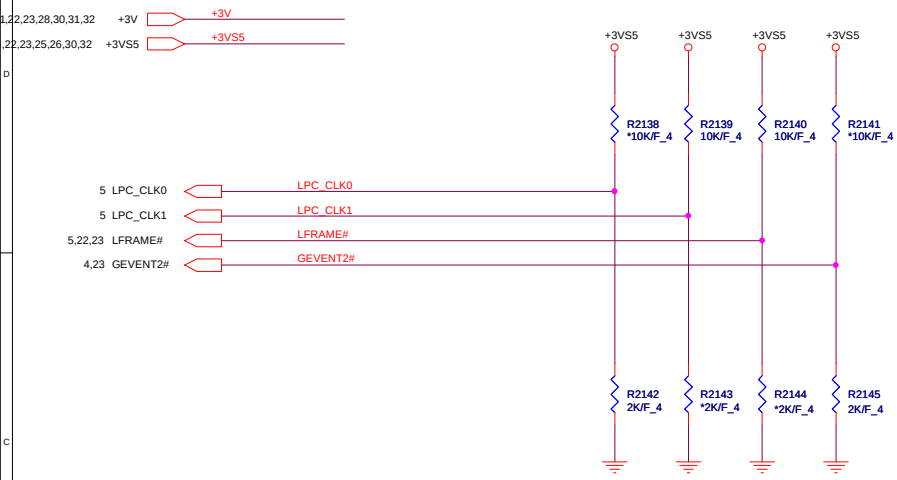






RAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



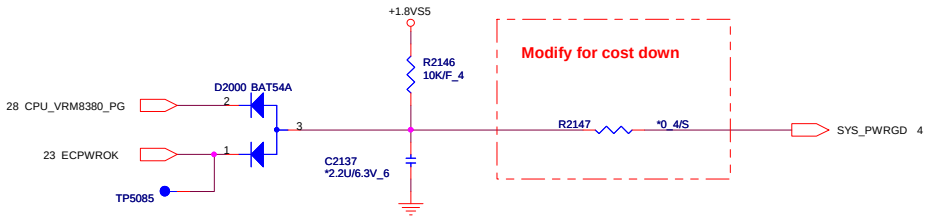
REQUIRED STRAPS

					LPC_CLK0	LPC_CLK1	LFRAME#	GEVENT2#
PULL HIGH					BOOT FAIL TIMER ENABLED	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM
PULL LOW					BOOT FAIL TIMER DISABLED DEFAULT	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM DEFAULT

DEBUG STRAPS

07

SYS PWRGD



PROJECT :U93
Quanta Computer Inc.

Size	Document Number	Rev
	STRAP (6/6)	1A

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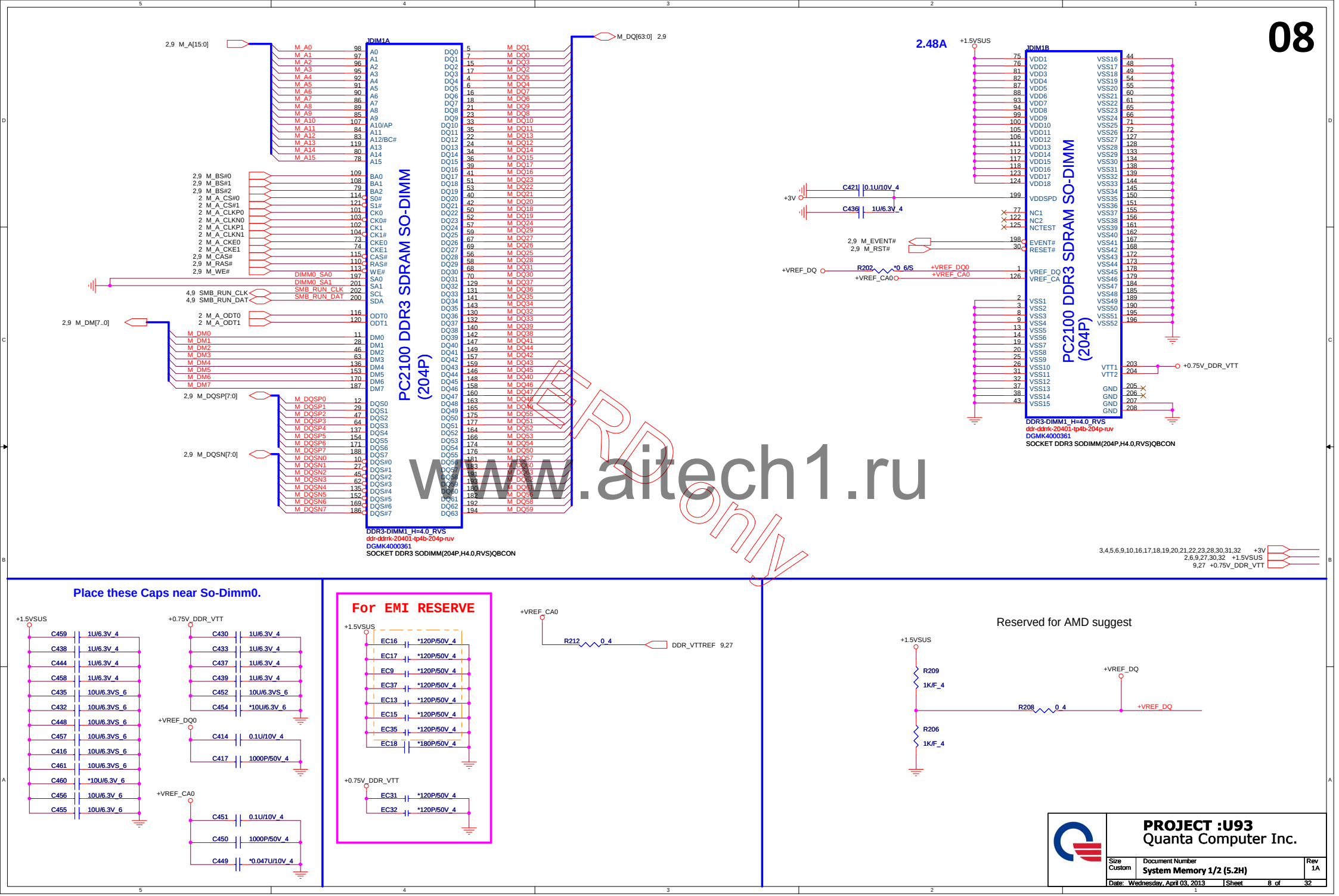


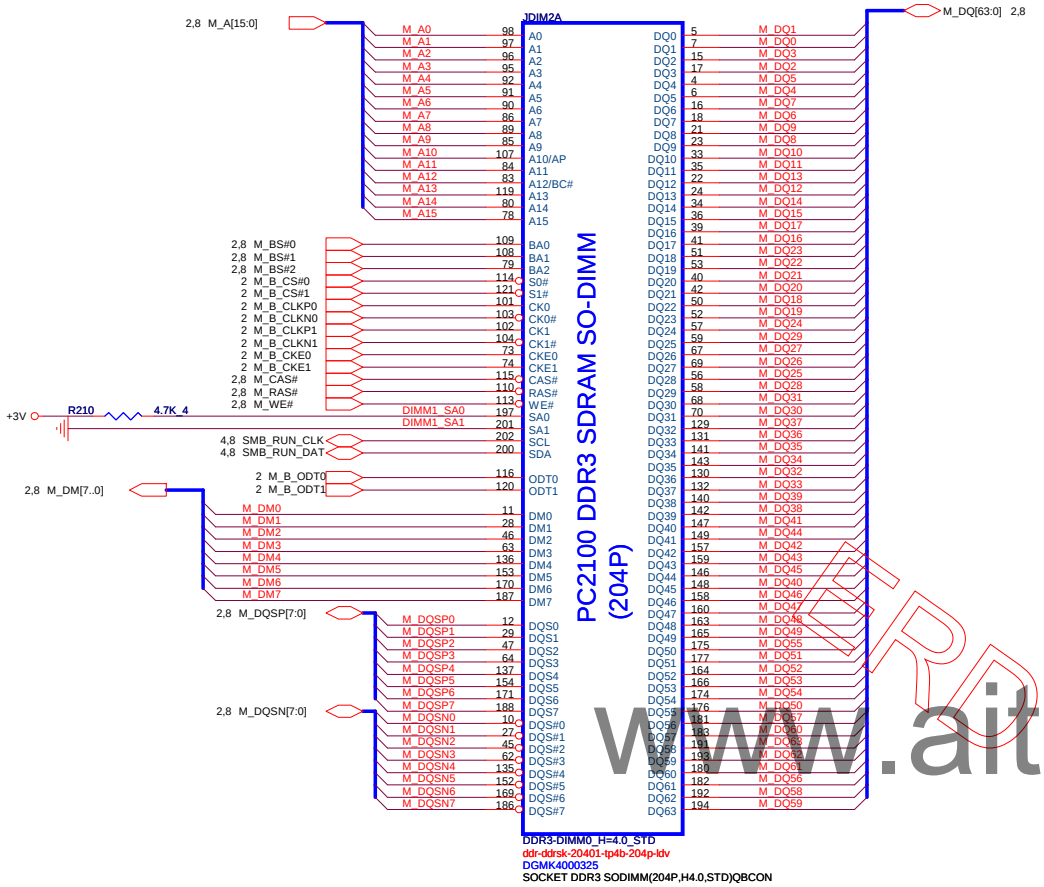
Place these Caps near So-Dimm0.

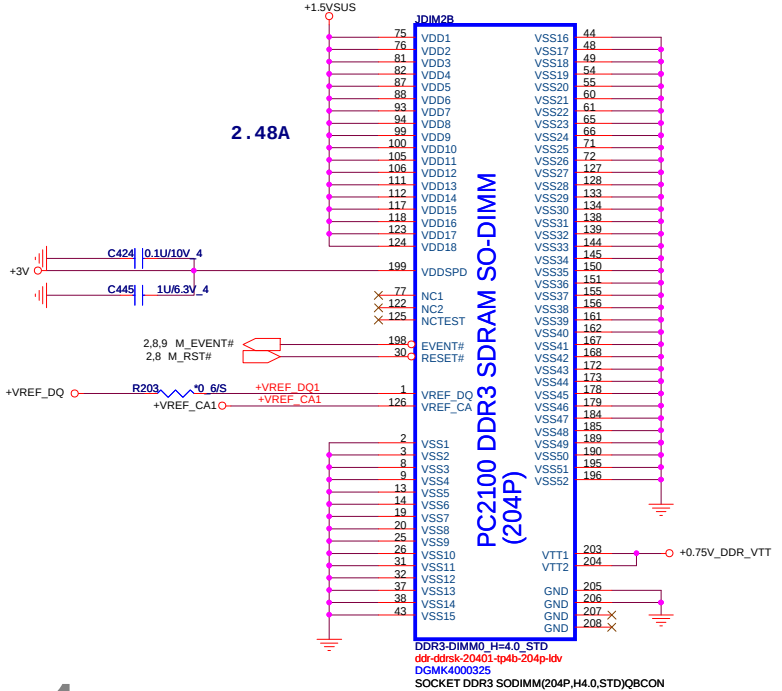
For EMI RESERVE

Reserved for AMD suggest

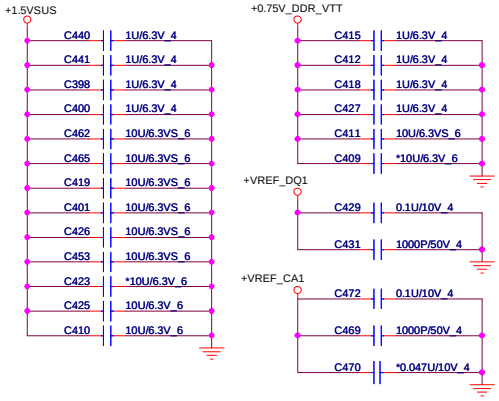
PROJECT :U93
Quanta Computer Inc.

Size	Document Number	Rev
Custom	System Memory 1/2 (5.2H)	1A
Date: Wednesday, April 03, 2013	Sheet 8 of 32	



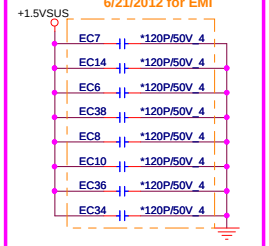


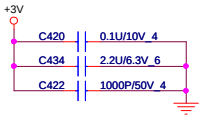
Place these Caps near So-Dimm1.



For EMI RESERVE

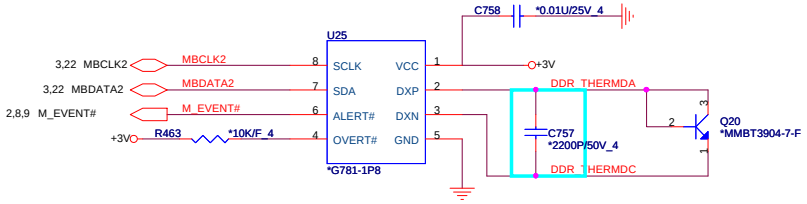
6/21/2012 for EMI





Local Thermal Sensor

DDR3 Thermal Sensor

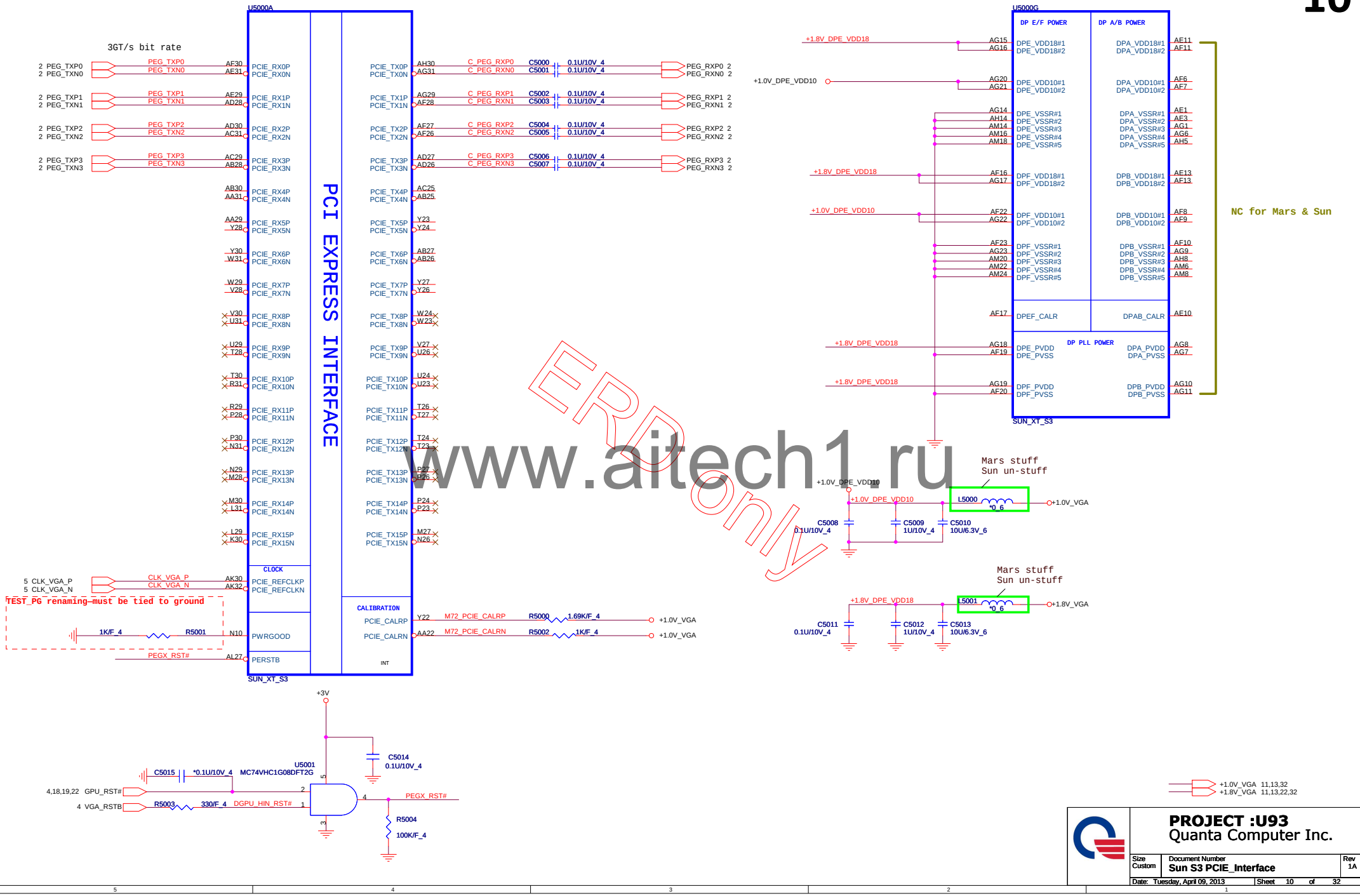


If use internal thermal IC, C9007 use 0ohm.

Main:AL000781039	G781-1P8(9Ah)
2nd:AL001412005	EMC1412-2-ACZL-TR(9Ah)
Main:AL001412003	EMC1412-1-ACZL-TR(98h)
2nd:AL000431014	TMP431ADGKR(98h)

PROJECT :U93
Quanta Computer Inc.

Size	Document Number	Rev
Custom	System Memory 2/2 (9.2H)	1A
Date: Wednesday, April 03, 2013	Sheet 9 of 32	



PROJECT :U93		
Quanta Computer Inc.		
Size: Custom	Document Number: Sun S3 PCIE_Interface	Rev: 1A
Date: Tuesday, April 09, 2013	Sheet 10 of 32	

GPIO10	GPIO30	GPIO16	GPIO20	GPIO15	Sun XT S3
PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	0	1	1.175V
0	1	1	1	0	1.150V
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Thermal Solution(Close to GPU)

Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)

MLPS Implementation
- Connect GPIO_28 to 10K pulldown to enable MLPS
- If any of PS_0/1/2/3 is not used, leave "no connect"
- R_pu, R_pd and C must be properly populated per tables below
- Place MLPS circuit components as close to the ASIC as possible
- Total DC resistance of trace between PS pin and C should be less than 2 ohms
- Total DC resistance of trace between C and ground should be less than 2 ohms
- Trace capacitance should be less than 100pF. Resistors should be of +/-1% tolerance

Capacitor Lookup Table

C (nF)	Bits(5,4)
680	00
82	01
10	10
NC	11

Resistor Divider Lookup Table

R_pu (Ohm)	R_pd (Ohm)	Bits(3,2,1)
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Pin/Bit	Name	Description	Default	Legacy
PS_0[3:1]	romidcfg[2:0]	Memory aperture size or ROM type select: If bios_rom_en = 0, romidcfg[2:0] define memory aperture size If bios_rom_en = 1, romidcfg[2:0] define ROM type	xxx	gpio_13 gpio_12 gpio_11
PS_0[4]	n/a	Reserved	1	genlk_vsync
PS_1[1]	bif_gen3_en_a	PCIe Gen3 capability: 1=Gen3 supported, 0=Gen3 not supported	x	gpio_2
PS_1[2]	bif_clk_pm_en	PCIe Clk PM capability: 1 = CLKREQB supported	x	gpio_8
PS_1[3]	n/a	Reserved		genlk_clk
PS_1[4]	tx_pwrs_enb	PCIe Tx power savings: 0=50% swing, 1=full swing	x	gpio_0
PS_1[5]	tx_deemph_en	PCIe Tx de-emphasis: 1=Tx de-emphasis enabled	x	gpio_1
PS_2[1]	n/a	Reserved		n/a
PS_2[2]	n/a	Reserved		n/a
PS_2[3]	bios_rom_en	Enable external BIOS ROM: 1=External ROM connected	x	gpio_22
PS_2[4]	vga_dis	VGA disable: 1=Disable this GPU as the system's VGA controller	0	gpio_9
PS_2[5]	n/a	Reserved		n/a
PS_3[1]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[2]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[3]	MEM Vendor ID	MEM Vendor ID	0	n/a
PS_3[5] PS_3[4] PS_0[5]	aud_port_cp[2] aud_port_cp[1] aud_port_cp[0]	3-bit field indicating number of audio-capable display outputs	xxx	n/a

PS_3[3:1]	Vendor	Type	Vendor P/N	R5045	R5048
000	Hynix- F(Huma)	128Mx16 *4, 900Mhz	H5TC2G63FFR-11C	NC	4.75K
001	Micron- V89C/K	128Mx16 *4, 800Mhz	MT41J128M16JT-093G:K	8.45K	2K
010	Samsung- E die	128Mx16 *4, 900Mhz	K4W2G1646E-BC1A	4.53K	2K
011	Hynix- Huma die	256Mx16 *4, 900Mhz	H5TC4G63FAFR-11C	6.98K	4.99K
100	Samsung- B die	256Mx16 *4, 900Mhz	K4W4G1646B-HC1A	4.53K	4.99K
101	Micron- E	256Mx16 *4, 900Mhz	MT41J256M16HA-093G:E	3.24K	5.62K

BIT5 => BIT0
PS0 => 11001
PS1 => 01000
PS2 => 00000
PS3 => 11000

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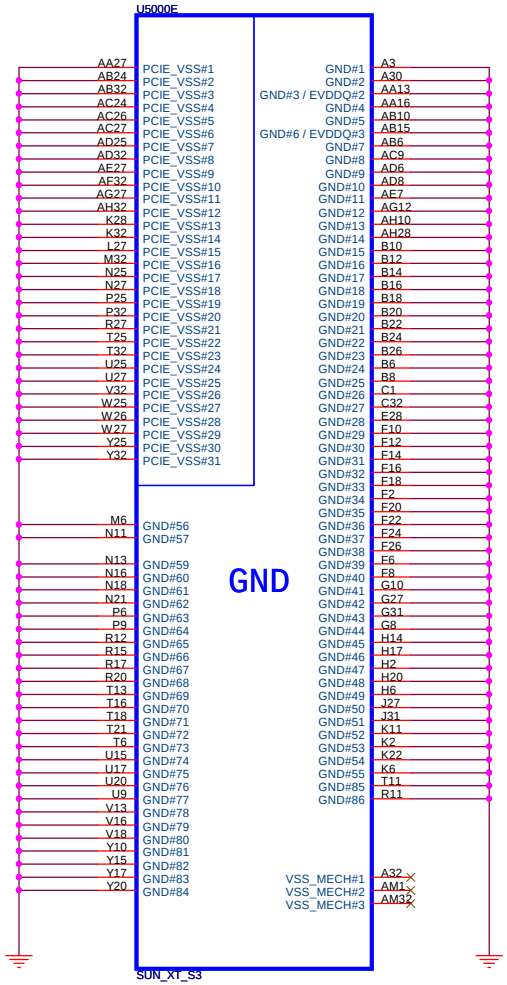
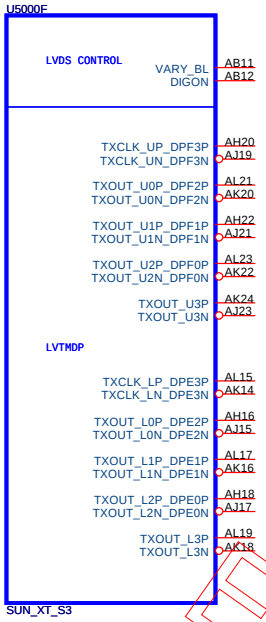
Quanta Computer Inc.
Size: Custom | Document Number: Sun S3 Main | Rev: 1A
Date: Wednesday, April 03, 2013 | Sheet 11 of 32





CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

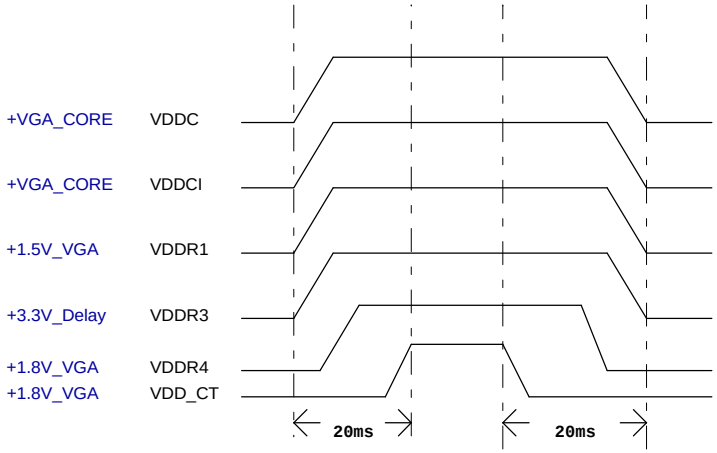
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	0 X
RSVD RSVD	GPIO2 GPIO8	RESERVED RESERVED	0 0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

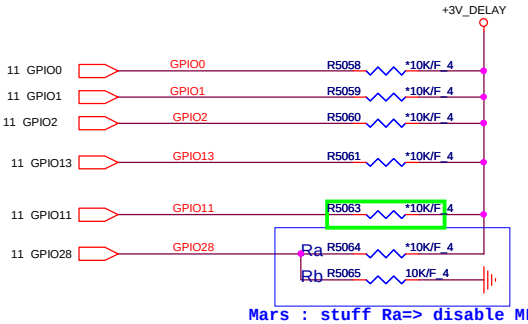
Power Up/Down Sequence



Memory Aperture size(Seymour)

GPIO9 BIOSROM		GPIO13 ROMIDCFG2	GPIO12 ROMIDCFG1	GPIO11 ROMIDCFG0
0	128M	0	0	0
0	256M	0	0	1
0	64M	0	1	0
0	32M	0	1	1
0	512M	1	0	0
0	1G	1	0	1
0	2G	1	1	0
0	4G	1	1	1

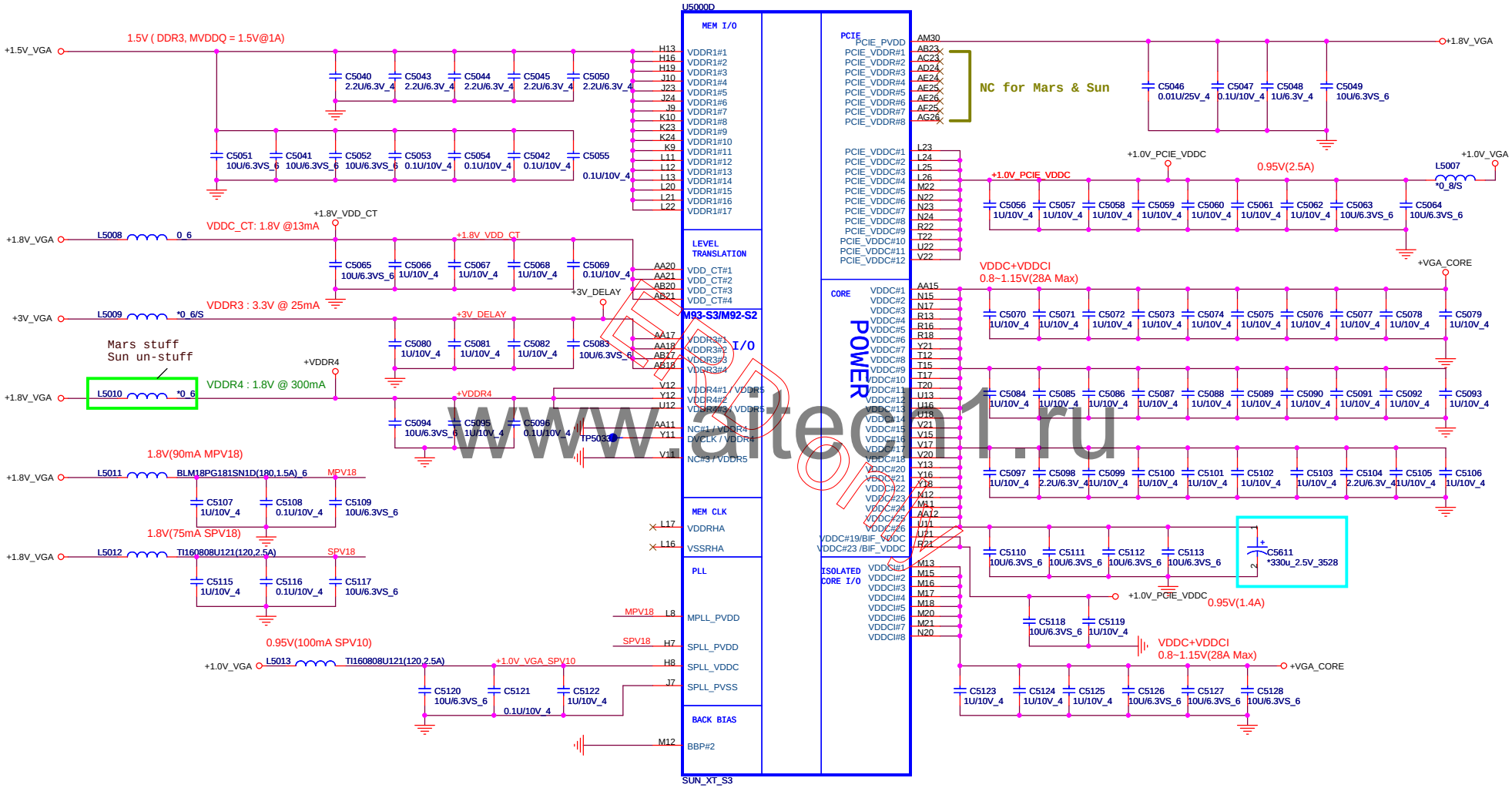
It is a shared pin strap with CONFIG[2:0] if BIOS_ROM_EN is set to 0.



+3V_DELAY 11,13

PROJECT :U93
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Sun S3 GND / LVDS/ Straps	1A
Date: Wednesday, April 03, 2013	Sheet 12 of 32	



PROJECT :U93 Quanta Computer Inc.		
Size: Custom	Document Number: Sun S3 Power_and_NC	Rev: 1A
Date: Wednesday, April 03, 2013	Sheet 13 of 32	

15 VMA_ODT0 → VMA_ODT0
15 VMA_ODT1 → VMA_ODT1
15 VMA_RAS0# → VMA_RAS0#
15 VMA_RAS1# → VMA_RAS1#
15 VMA_CAS0# → VMA_CAS0#
15 VMA_CAS1# → VMA_CAS1#
15 VMA_WE0# → VMA_WE0#
15 VMA_WE1# → VMA_WE1#
15 VMA_CS0# → VMA_CS0#
15 VMA_CS1# → VMA_CS1#
15 VMA_CKE0 → VMA_CKE0
15 VMA_CKE1 → VMA_CKE1
15 VMA_CLK0 → VMA_CLK0
15 VMA_CLK0# → VMA_CLK0#
15 VMA_CLK1 → VMA_CLK1
15 VMA_CLK1# → VMA_CLK1#
15 VMA_WDQS[7..0] → VMA_WDQS[7..0]
15 VMA_RDQS[7..0] → VMA_RDQS[7..0]
15 VMA_DM[7..0] → VMA_DM[7..0]
15 VMA_DQ[63..0] → VMA_DQ[63..0]
15 VMA_MA[14..0] → VMA_MA[14..0]
15 VMA_BA0 → VMA_BA0
15 VMA_BA1 → VMA_BA1
15 VMA_BA2 → VMA_BA2

support 1Gbit VRAM (64M X 16)

U5000C

MEMORY INTERFACE

VMA_DQ0	K27	DQA_0	
VMA_DQ1	J29	DQA_1	
VMA_DQ2	H30	DQA_2	
VMA_DQ3	H32	DQA_3	
VMA_DQ4	G29	DQA_4	
VMA_DQ5	F28	DQA_5	
VMA_DQ6	F32	DQA_6	
VMA_DQ7	F30	DQA_7	
VMA_DQ8	C30	DQA_8	
VMA_DQ9	F27	DQA_9	
VMA_DQ10	A28	DQA_10	
VMA_DQ11	C28	DQA_11	
VMA_DQ12	E27	DQA_12	
VMA_DQ13	G26	DQA_13	
VMA_DQ14	D26	DQA_14	
VMA_DQ15	F25	DQA_15	
VMA_DQ16	A25	DQA_16	
VMA_DQ17	C25	DQA_17	
VMA_DQ18	E25	DQA_18	
VMA_DQ19	D24	DQA_19	
VMA_DQ20	E23	DQA_20	
VMA_DQ21	F23	DQA_21	
VMA_DQ22	D22	DQA_22	
VMA_DQ23	F21	DQA_23	
VMA_DQ24	E21	DQA_24	
VMA_DQ25	D20	DQA_25	
VMA_DQ26	F19	DQA_26	
VMA_DQ27	A19	DQA_27	
VMA_DQ28	D18	DQA_28	
VMA_DQ29	F17	DQA_29	
VMA_DQ30	A17	DQA_30	
VMA_DQ31	C17	DQA_31	
VMA_DQ32	E17	DQA_32	
VMA_DQ33	D16	DQA_33	
VMA_DQ34	F15	DQA_34	
VMA_DQ35	A15	DQA_35	
VMA_DQ36	D14	DQA_36	
VMA_DQ37	F13	DQA_37	
VMA_DQ38	A13	DQA_38	
VMA_DQ39	C13	DQA_39	
VMA_DQ40	E11	DQA_40	
VMA_DQ41	A11	DQA_41	
VMA_DQ42	C11	DQA_42	
VMA_DQ43	F11	DQA_43	
VMA_DQ44	A9	DQA_44	
VMA_DQ45	C9	DQA_45	
VMA_DQ46	F9	DQA_46	
VMA_DQ47	D8	DQA_47	
VMA_DQ48	E7	DQA_48	
VMA_DQ49	A7	DQA_49	
VMA_DQ50	C7	DQA_50	
VMA_DQ51	F7	DQA_51	
VMA_DQ52	A5	DQA_52	
VMA_DQ53	E5	DQA_53	
VMA_DQ54	C3	DQA_54	
VMA_DQ55	F1	DQA_55	
VMA_DQ56	G7	DQA_56	
VMA_DQ57	G6	DQA_57	
VMA_DQ58	G1	DQA_58	
VMA_DQ59	G3	DQA_59	
VMA_DQ60	J6	DQA_60	
VMA_DQ61	J1	DQA_61	
VMA_DQ62	J3	DQA_62	
VMA_DQ63	J5	DQA_63	

MAA_0	K17	VMA_MA0	
MAA_1	J20	VMA_MA1	
MAA_2	H23	VMA_MA2	
MAA_3	G23	VMA_MA3	
MAA_4	G24	VMA_MA4	
MAA_5	H24	VMA_MA5	
MAA_6	J19	VMA_MA6	
MAA_7	K19	VMA_MA7	
MAA_8	J14	VMA_MA8	
MAA_9	K14	VMA_MA9	
MAA_10	J11	VMA_MA10	
MAA_11	J13	VMA_MA11	
MAA_12	H11	VMA_MA12	
MAA_13/BA2	G11	VMA_BA2	
MAA_14/BA0	J16	VMA_BA0	
MAA_15/BA1	L15	VMA_BA1	
DQMA_0	E32	VMA_DM0	
DQMA_1	E30	VMA_DM1	
DQMA_2	A21	VMA_DM2	
DQMA_3	C21	VMA_DM3	
DQMA_4	E13	VMA_DM4	
DQMA_5	D12	VMA_DM5	
DQMA_6	E3	VMA_DM6	
DQMA_7	F4	VMA_DM7	
RDQSA_0	H28	VMA_RDQS0	
RDQSA_1	C27	VMA_RDQS1	
RDQSA_2	A23	VMA_RDQS2	
RDQSA_3	E19	VMA_RDQS3	
RDQSA_4	E15	VMA_RDQS4	
RDQSA_5	D10	VMA_RDQS5	
RDQSA_6	D6	VMA_RDQS6	
RDQSA_7	G5	VMA_RDQS7	
WDQSA_0	H27	VMA_WDQS0	
WDQSA_1	A27	VMA_WDQS1	
WDQSA_2	C23	VMA_WDQS2	
WDQSA_3	C19	VMA_WDQS3	
WDQSA_4	C15	VMA_WDQS4	
WDQSA_5	E9	VMA_WDQS5	
WDQSA_6	C5	VMA_WDQS6	
WDQSA_7	H4	VMA_WDQS7	
ODTA0	L18	VMA_ODT0	
ODTA1	K16	VMA_ODT1	
CLKA0	H26	VMA_CLK0	
CLKA0B	H25	VMA_CLK0#	
CLKA1	G9	VMA_CLK1	
CLKA1B	H9	VMA_CLK1#	
RASA0B	G22	VMA_RAS0#	
RASA1B	G17	VMA_RAS1#	
CASA0B	G19	VMA_CAS0#	
CASA1B	G16	VMA_CAS1#	
CSA0B_0	H22	VMA_CS0#	
CSA0B_1	J22		
CSA1B_0	G13	VMA_CS1#	
CSA1B_1	K13		
CKEA0	K20	VMA_CKE0	
CKEA1	J17	VMA_CKE1	
WEA0B	G25	VMA_WE0#	
WEA1B	H10	VMA_WE1#	
PX_EN	AB16	PX_EN	
RSVD#2	G14	VMA_MA14	
RSVD#3	G20	VMA_MA13	

K26	MVREFDA		
J26	MVREFSA		
J25	MEM_CALRN0		
K7	NC/TESTEN#2		
J8	MEM_CALRP1/DPC_CALR		
K25	MEM_CALRP0		
L10	DRAM_RST		
K8	CLKTESTA		
L7	CLKTESTB		

SUN_XT_S3

PX_EN → TP5034

+1.5V_VGA
R5069 40.2/F_4
MVREFD
R5070 400/F_4
C5130 1U/10V_4
+1.5V_VGA
R5072 40.2/F_4
MVREFS
C5131 1U/10V_4
R5074 100/F_4

R5071 1K/F_4
R5073 120/F_4

DRAM_RST
CLKTESTA
CLKTESTB

C5132 *0.1U/10V_4
C5133 *0.1U/10V_4
R5075 *51.1/F_4
R5076 *51.1/F_4

route 50ohms single-ended/100ohms diff and keep short

From GPU
25mm (max) 5mm (max) 25mm (max)
DRAM_RST → R5066 10/F_4 → R5067 51.1/F_4 → DRAM_RST_M → DRAM_RST_M 15
R5068 4.99K/F_4
C5129 120P/50V_4

Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

+1.5V_VGA 13,15,32

PROJECT :U93
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Sun S3 MEM_Interface	1A

Date: Wednesday, April 03, 2013 | Sheet 14 of 32

1G DDR3

14 VMA_MA[14..0]
14 VMA_DM[7..0]
VMA_MA[14..0]
14 VMA_DQ[63..0]
14 VMA_WDQS[7..0]
14 VMA_RDQS[7..0]

U5003 / U5004 / U5005 / U5006

100-BALL SDRAM DDR3
K4W2G1646E-BC1A

+1.5V_VGA

Should be 240 Ohms +-1%

R5077 243/F_4
R5078 243/F_4
R5079 243/F_4
R5080 243/F_4

R5081 4.99K/F_4
R5082 4.99K/F_4
R5083 4.99K/F_4
R5084 4.99K/F_4
R5085 4.99K/F_4
R5086 4.99K/F_4
R5087 4.99K/F_4
R5088 4.99K/F_4
R5089 4.99K/F_4
R5090 4.99K/F_4
R5091 4.99K/F_4
R5092 4.99K/F_4
R5093 4.99K/F_4
R5094 4.99K/F_4
R5095 4.99K/F_4
R5096 4.99K/F_4

VREFC_VMA1 / VREFD_VMA1
VREFC_VMA2 / VREFD_VMA2
VREFC_VMA3 / VREFD_VMA3
VREFC_VMA4 / VREFD_VMA4

C5134 0.1U/10V_4
C5135 0.1U/10V_4
C5136 0.1U/10V_4
C5137 0.1U/10V_4
C5138 0.1U/10V_4
C5139 0.1U/10V_4
C5140 0.1U/10V_4
C5141 0.1U/10V_4

+1.5V_VGA 13,14,32

C5142 C5143 C5144 C5145 C5146 C5147 C5148 C5149 1U/6.3V_4
C5150 C5151 C5152 C5153 C5154 C5155 C5156 C5157 1U/6.3V_4
C5159 C5160 C5161 C5162 C5163 C5164 C5165 C5166 1U/6.3V_4
C5167 C5168 C5169 C5170 C5171 C5172 C5173 C5174 1U/6.3V_4
C5176 C5177 C5178 C5179 C5180 10U/6.3VS_6
C5181 C5182 C5183 C5184 C5185 C5186 C5187 10U/6.3VS_6

VMA_CLK0
VMA_CLK0#
VMA_CLK1
VMA_CLK1#
R5097 40.2/F_4
R5098 40.2/F_4
R5099 40.2/F_4
R5100 40.2/F_4
VMA_CLK0_COMM
VMA_CLK1_COMM
C5158 0.01U/25V_4
C5175 0.01U/25V_4

	TOPBSQ_PN
Hynix	AKD5MGWTW13
Micron	AKD5MGSTL08
SAMSUNG	AKD5MGGT522

PROJECT :U93
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Sun S3 VRAM(DDR3 BGA96P)	1A

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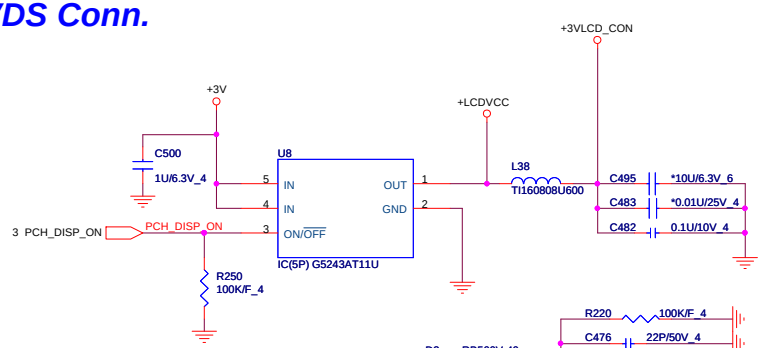
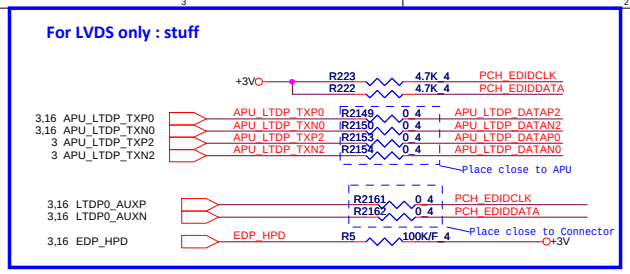
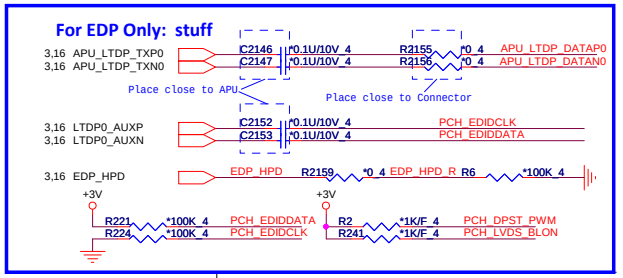
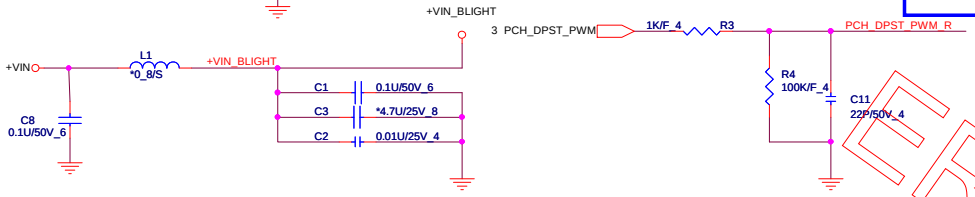
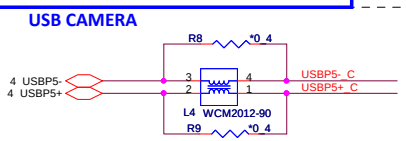
LVDS Conn.

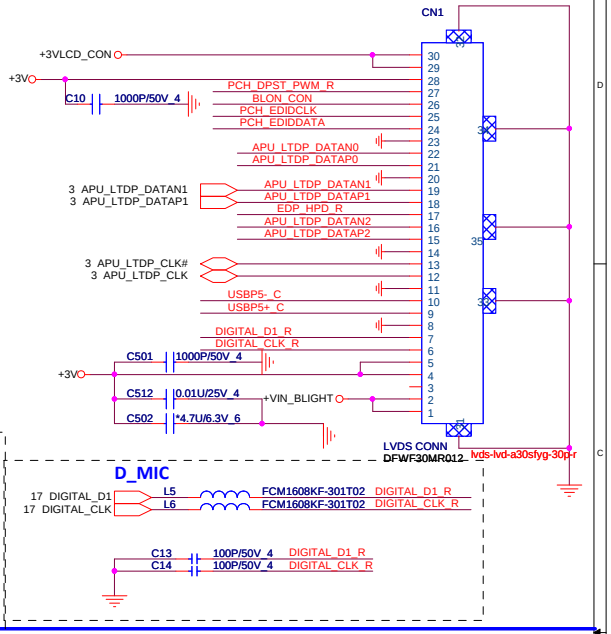






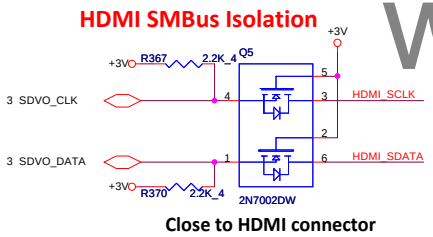


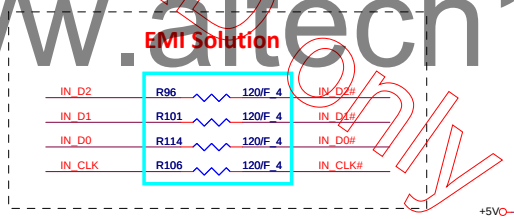


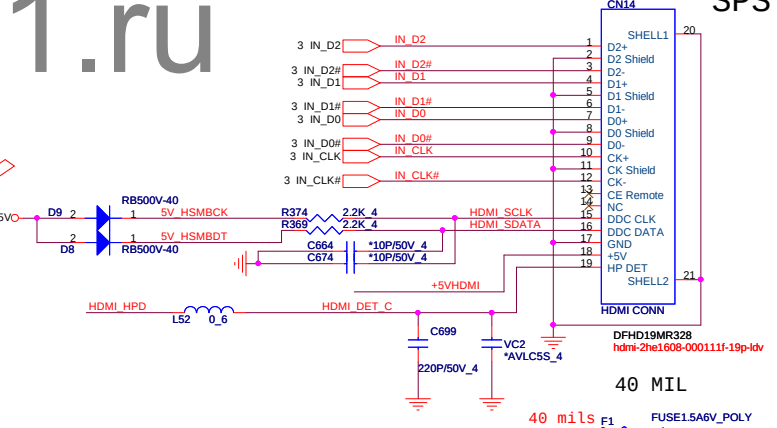


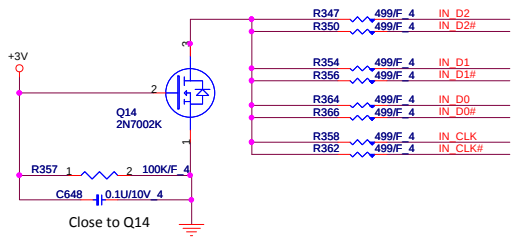
HDMI Conn.

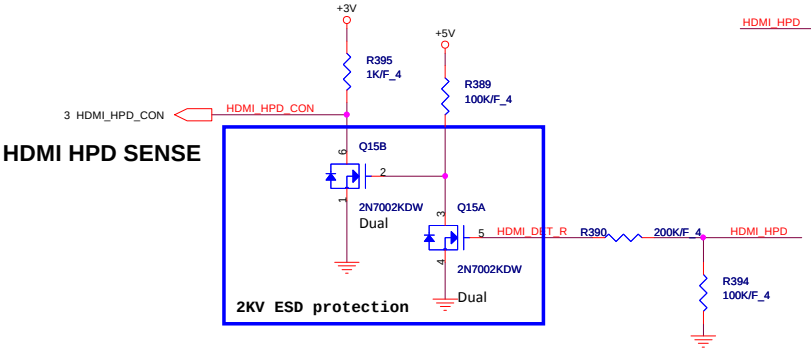
SPS Type

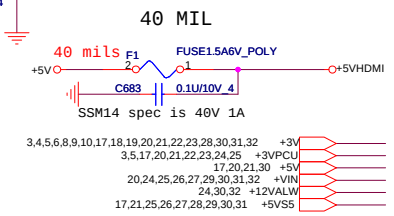












3,4,5,6,8,9,10,17,18,19,20,21,22,23,28,30,31,32 +3V
3,5,17,20,21,22,23,24,25 +3VPCU
17,20,21,30 +5V
20,24,25,26,27,29,30,31,32 +VIN
24,30,32 +12VALW
17,21,25,26,27,28,29,30,31 +5VS5

PROJECT :U93
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD Connector (LVDS)	1A
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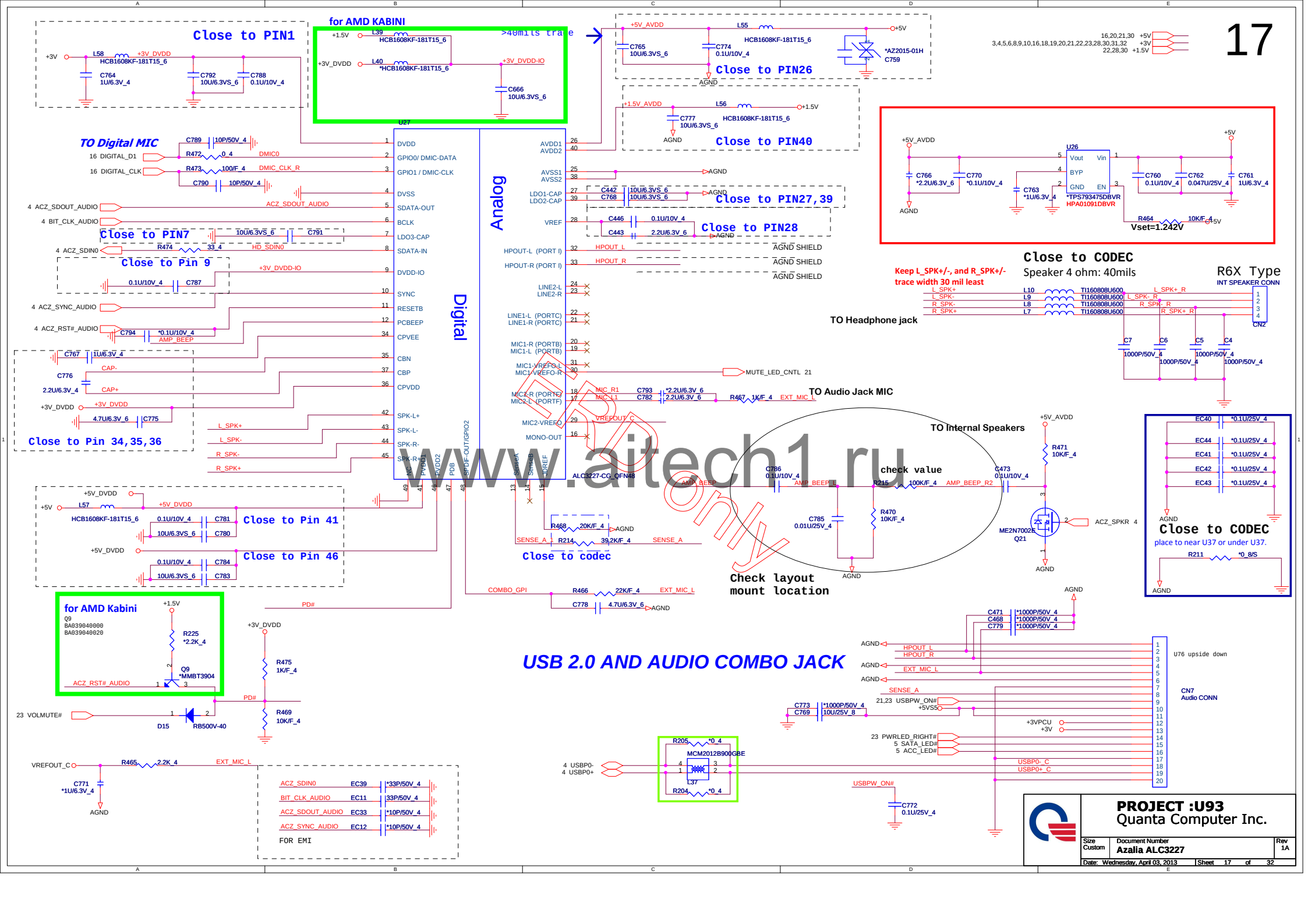
17
Close to PIN1
for AMD KABINI
>40mils trace
Close to PIN26
Close to PIN40
Close to PIN27,39
Close to PIN28
Close to CODEC
Speaker 4 ohm: 40mils
R6X Type
INT SPEAKER CONN
Keep L_SPK+/-, and R_SPK+/- trace width 30 mil least
TO Digital MIC
TO Headphone jack
TO Audio Jack MIC
TO Internal Speakers
Close to PIN7
Close to Pin 9
Close to Pin 34,35,36
Close to Pin 41
Close to Pin 46
Close to codec
check value
Check layout
mount location
for AMD Kabini
USB 2.0 AND AUDIO COMBO JACK
Close to CODEC
place to near U37 or under U37.
Analog
Digital
U27
ALC3227-CG_QFN48
U26
TPS793475DBVR
HPA01091DBVR
Vset=1.242V
ME2N7002E
Q21
CN7
Audio CONN
U76 upside down
MCM2012B900GBE
RB500V-40
D15
FOR EMI
PROJECT :U93
Quanta Computer Inc.
Azalia ALC3227
Size Custom
Document Number
Rev 1A
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www.aitech1.ru
only

For EMI 0 ~ 22 ohm

R42 10_4 LAN_XTAL1 XTAL1

R48 *0_4 LAN_XTAL25_IN 22

Y1 25MHZ +-10PPM XTAL2

C43 12P/50V_4 C39 12P/50V_4

SI change to 12p

>60mil Power trace Layout 寬度> 60mil

+1.05V_LAN_REGOUT C27 0.1U/10V_4 +1.05V_LAN

Place close PIN23 and PIN32

+3V_LAN +3VLANVCC C41 0.1U/10V_4 Ca C504 0.1U/10V_4 Cb

Place close PIN30

+1.05V_LAN C506 0.1U/10V_4 C510 1U/6.3V_4 C25 0.1U/10V_4

R45 2.49K/F_4 LANRSET

+3V_LAN R41 0_4 LAN_WLED#

LAN_ALED# P101 P102 P103

+3V R26 1K/F_4 ISOLATEB R27 15K/F_4

if ISOLATEB pin pull-low,the LAN chip will not drive it's PCI-E outputs (excluding PCIE_WAKE# pin)

U1 RTL 8166EH RTL8166EH-CG

Please add 9 GND VIAs connection with thermal PAD

Place close PIN8 C509 0.1U/10V_4

+3V R2114 10K/F_4

4 PCIE_CLKREQ_LAN# PCIE_CLKREQ_LAN# R254 0_4 LAN_CLKRQ

MDI0+ MDI0- MDI1+ MDI1- MDIP0 MDIN0 MDIP1 MDIN1 MDIP2(NC) MDIN2(NC) AVDD10(NC) VDD10

REGOUT(NC) VDDREG(VDD33) DVDD10(NC) LANWAKEB ISOLATEB PERSTB HSON HSOP

+1.05V_LAN_REGOUT +3V_LAN +1.05V_LAN PCIE_WAKE# 4,22 RLTRST# 4,10,19,22 PCIE_RXN1_LAN 2 PCIE_RXP1_LAN 2

C24 0.1U/10V_4 C22 0.1U/10V_4

CLK_PCIE_LANN CLK_PCIE_LANP PCIE_TXN1_LAN PCIE_TXP1_LAN

CLK_PCIE_LANN 5 CLK_PCIE_LANP 5 PCIE_TXN1_LAN 2 PCIE_TXP1_LAN 2

U9 NS681684

MDI1+_1 MDI1-_1 MDI0+_1 MDI0-_1 TD+ TD- CT RD+ RD- CT

CMT TX+ RX- CT RX+

MDI1+ MDI1- MDI0- MDI0+

V_DAC2 V_DAC1

75_4 R20 C800 0.01U/100V_6 LAN_MCT1

75_4 R28 C801 0.01U/100V_6 LAN_MCT0

C485 10P/3KV_1808 C528 0.01U/25V_4

LAN conn

RJ45 (White) CN11

LAN_WLED LAN_WLED# LED_WHITE_P LED_WHITE_N

RX1- RX1+ RX0- TX1- TX1+ RX0+ TX0- TX0+ GND1 GND

MDI1-_1 MDI1+_1 MDI0-_1 MDI0+_1

R1 *0_6/S R50 *0_6/S

LAN_ALED LAN_ALED# LED_AMBER_P LED_AMBER_N

(Amber) RJ-45

C498 68P/50V_4

Need Change PN/FP after DB

+3VLANVCC R49 330/F_4 C45 1000P/50V_4 LAN_ALED 朝前

+3VLANVCC R13 330/F_4 LAN_WLED C17 1000P/50V_4 朝前

3,4,5,6,8,9,10,16,17,19,20,21,22,23,28,30,31,32 +3V

22,30 +3VLANVCC

PROJECT :U93

Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTL 8166EH/RJ45	1A

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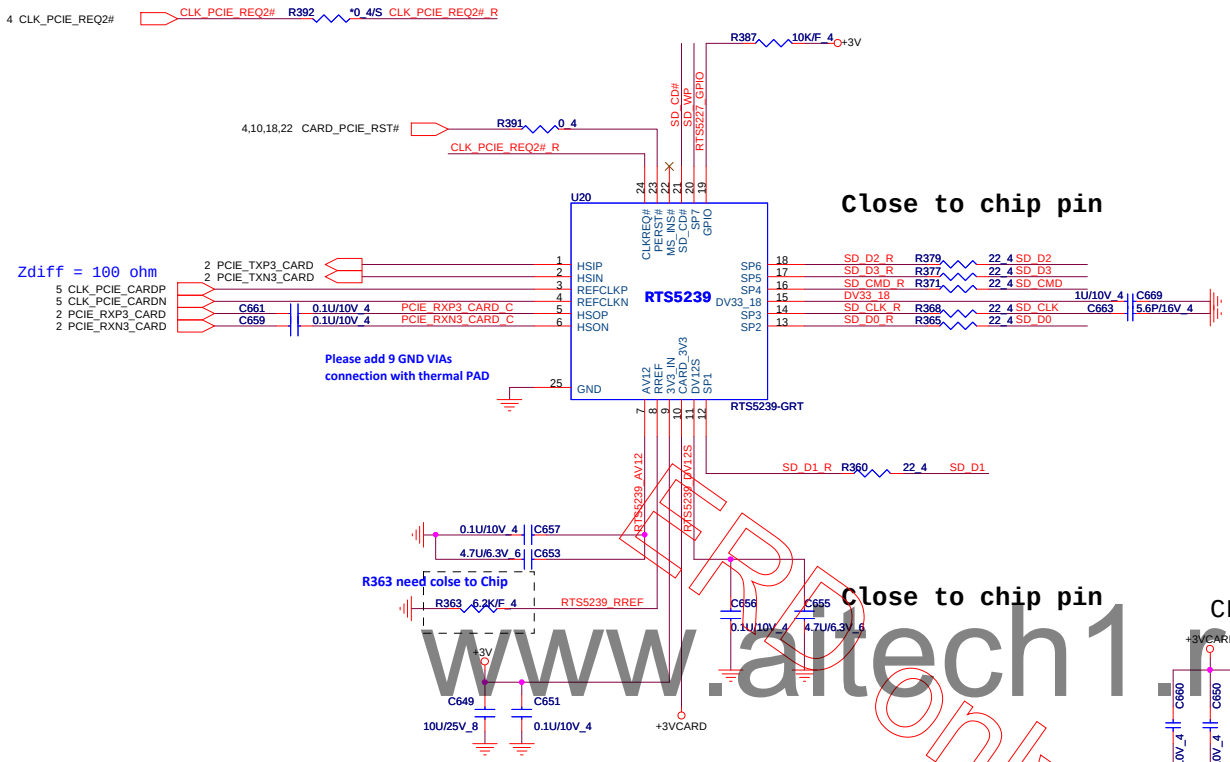
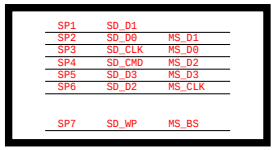
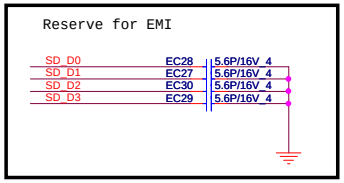
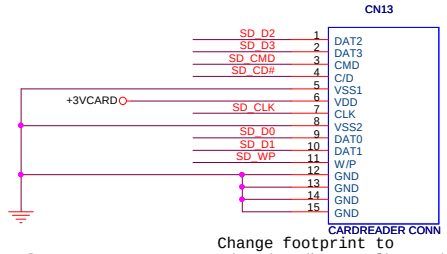




Share Pin



SD / MMC
CARD READER



Change footprint to
sdcard-psdbtc-09glbs1nn4h3-11p

R3X Type

PROJECT :U93
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5239 & CR SOCKET	1A
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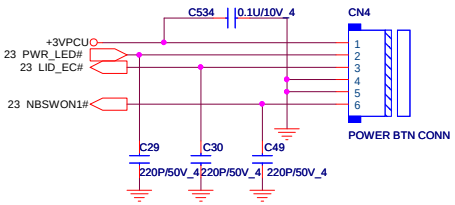
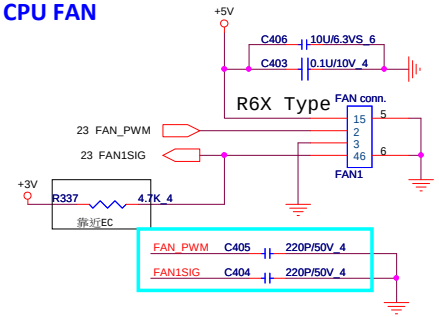
Power Botton Connector

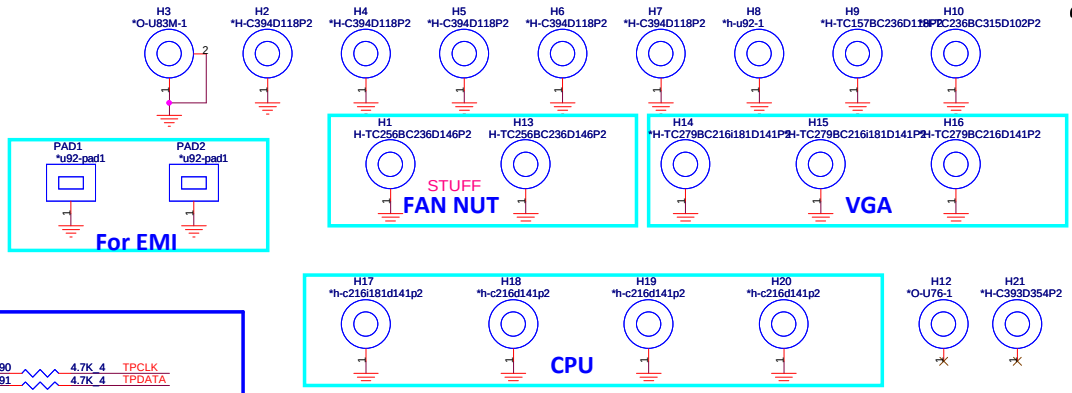
Pin1 : +3VPCU(LIDSWITCH PWR)
Pin2 : POWER LED
Pin3 : LIDSWITCH
Pin4 : GND
Pin5 : GND
Pin6 : POWERON#



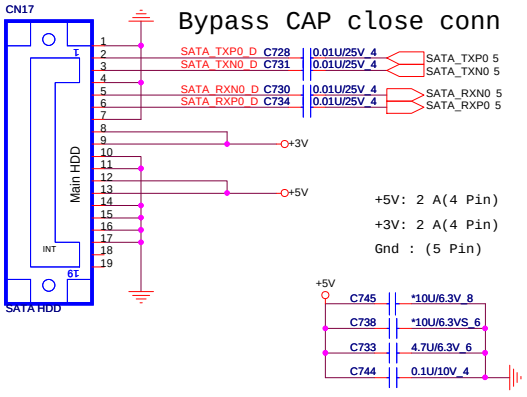
CPU FAN

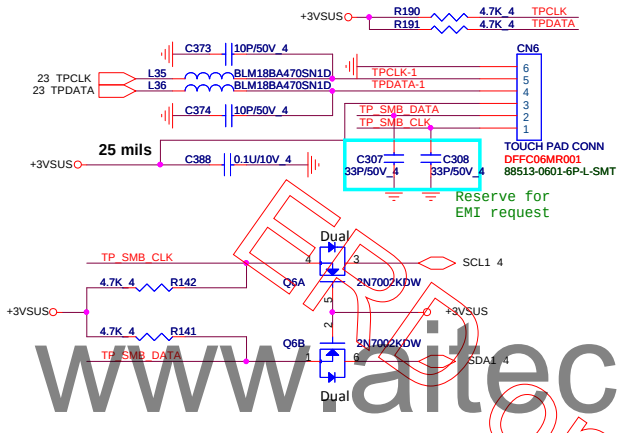


Hole

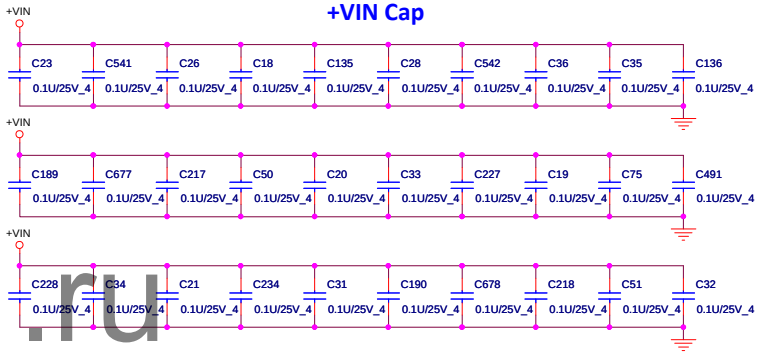


SATA HDD Connector(Cable type)





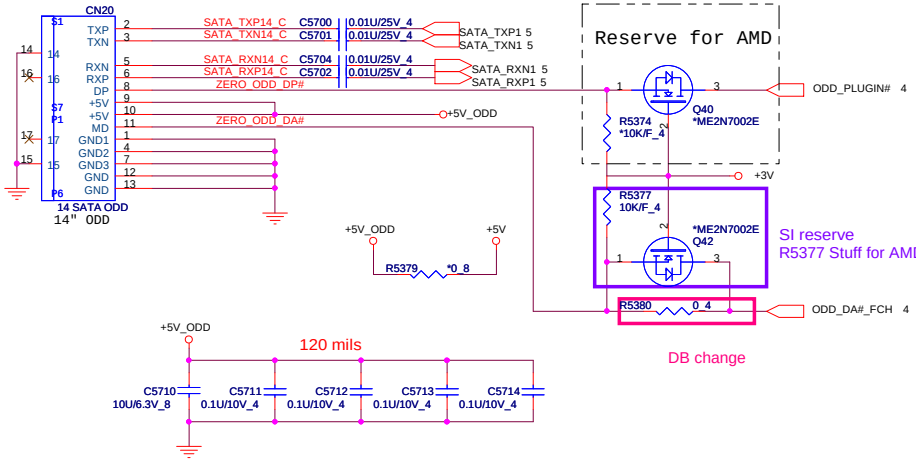
+VIN Cap

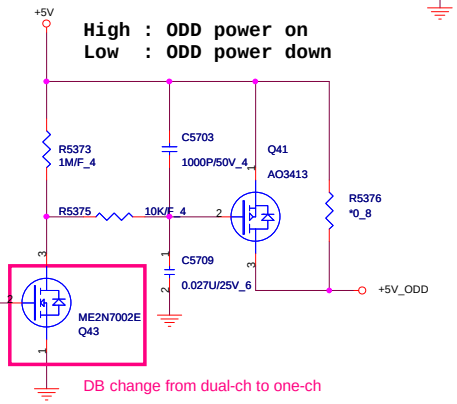


SATA ODD CONNECTOR

14" SATA ODD

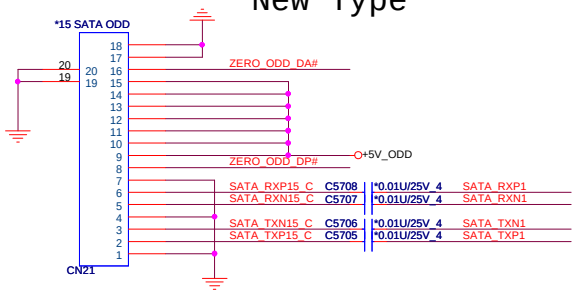
Bypass CAP close conn





15" SATA ODD

New Type



16,17,21,30 +5V
3,5,17,21,22,23,24,25 +3VPCU
17,22,28,30 +1.5V
24,30,32 +12VALW
3,4,5,6,8,9,10,16,17,18,19,21,22,23,28,30,31,32 +3V

PROJECT :U93
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD/ODD/MSATA CONN	1A
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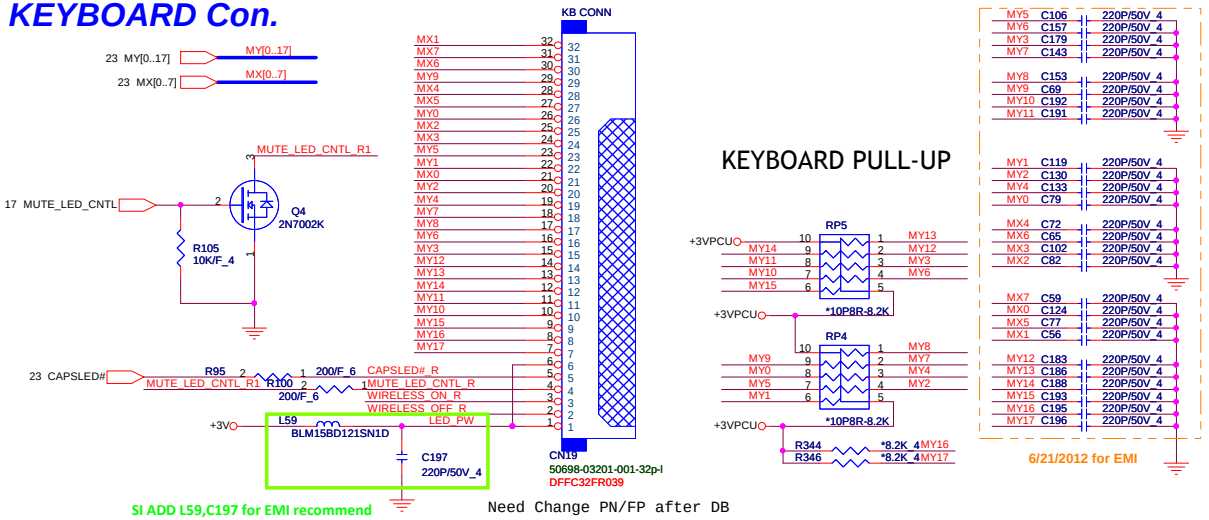
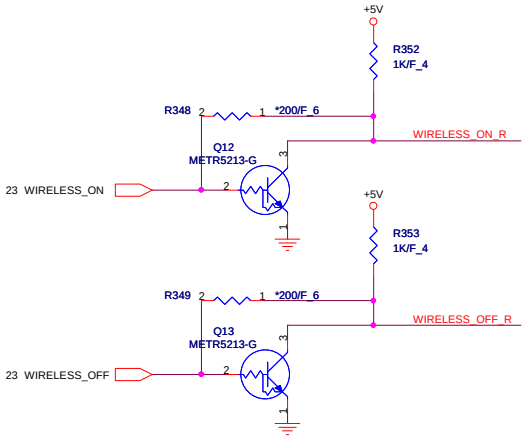
KEYBOARD Con.



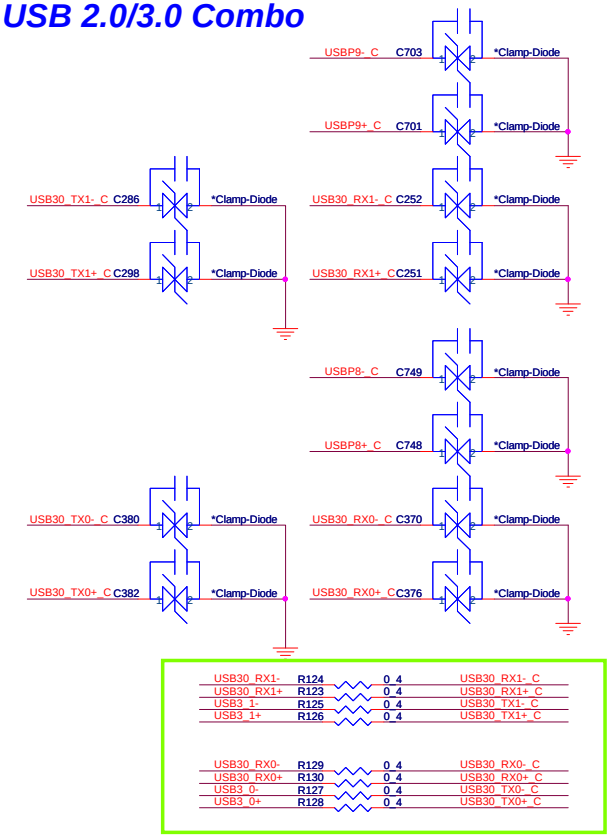
KEYBOARD PULL-UP



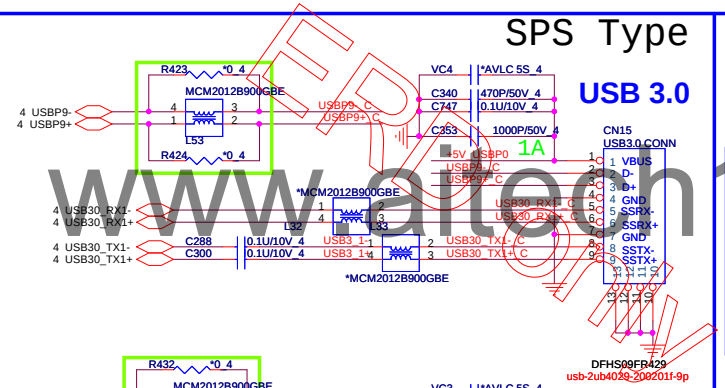
Need Change PN/FP after DB

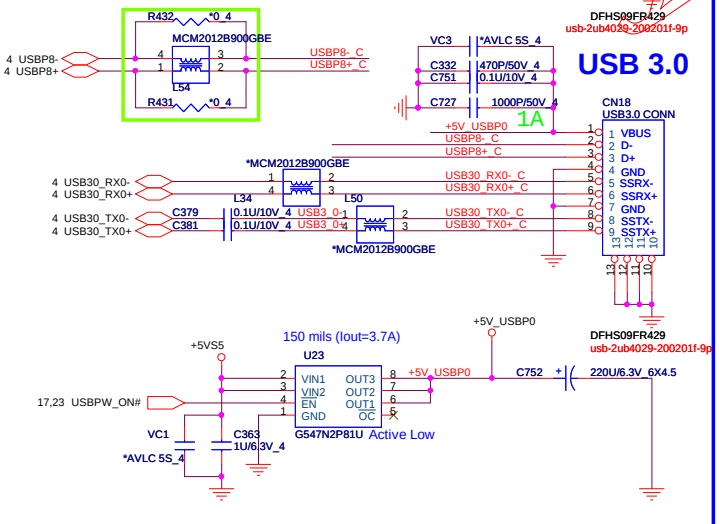
NM9 Type

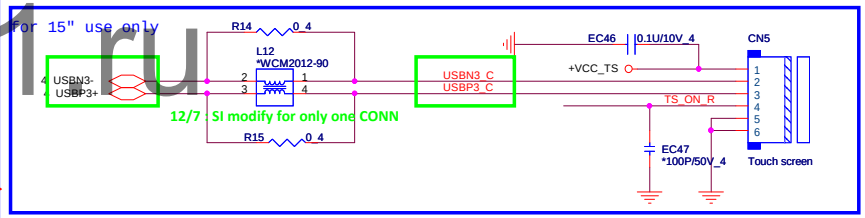
USB 2.0/3.0 Combo

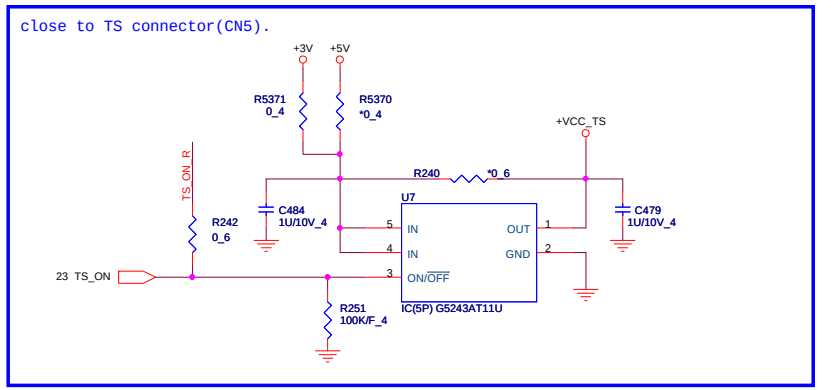


SPS Type









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Quanta Computer Inc.	
Size: Custom	Document Number: USB 3.0/KB/Green CLK
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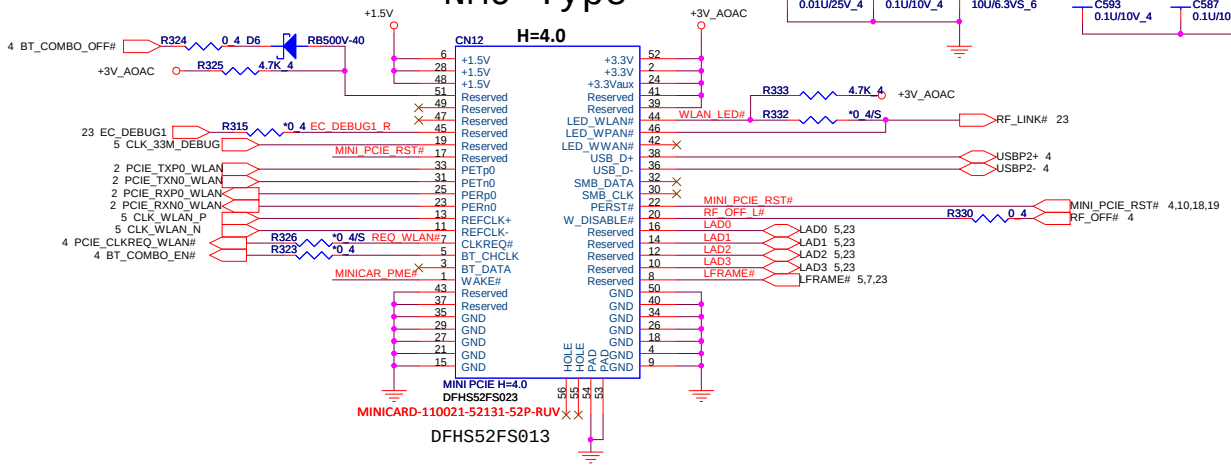
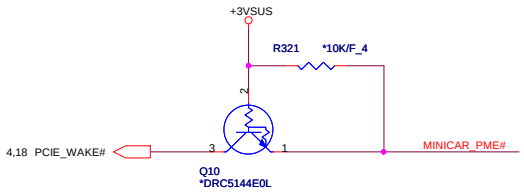
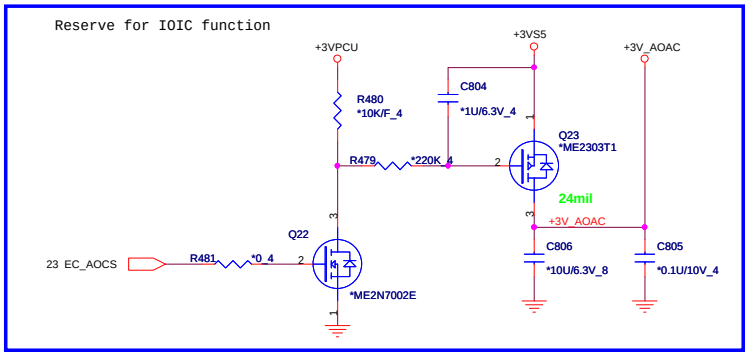
Date: Tuesday, April 09, 2013	Sheet: 21 of 32

Mini Card
WLAN/BT(Option)

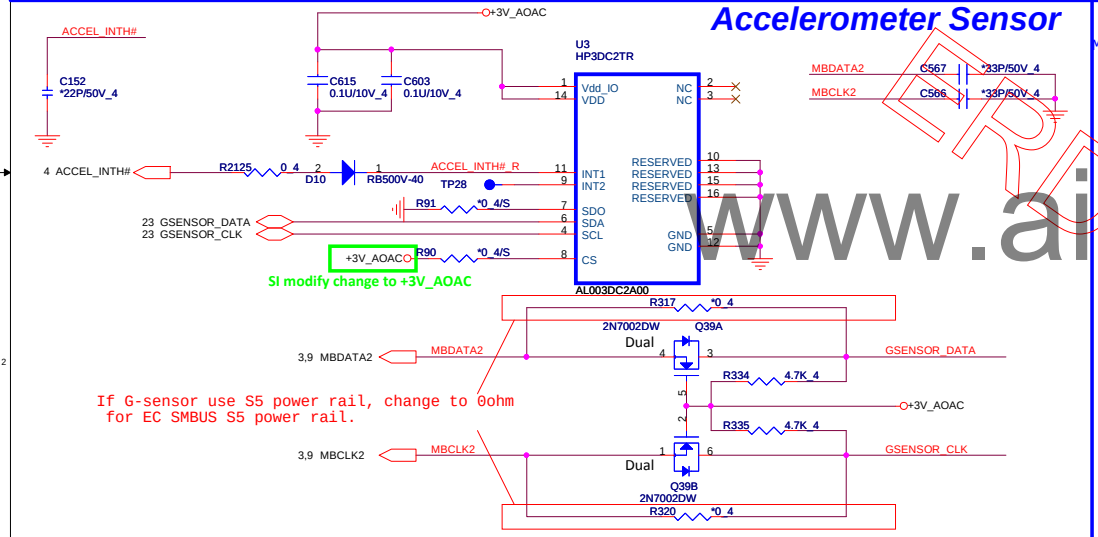
NM9 Type





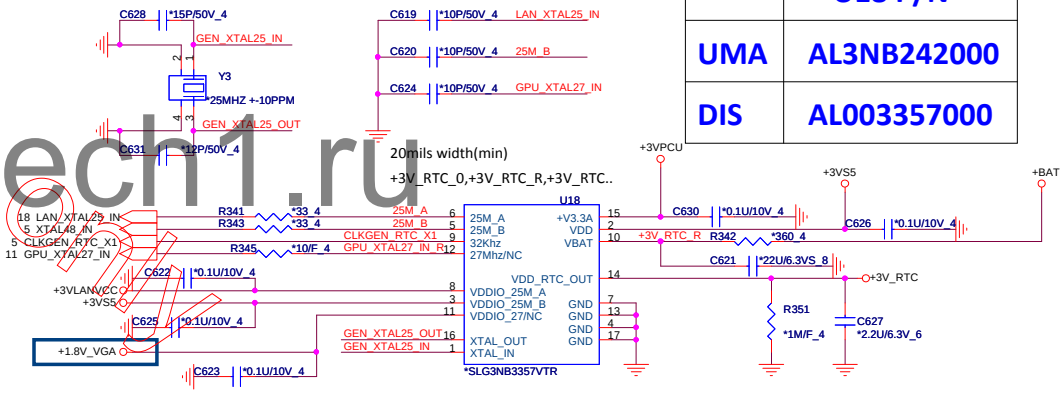


Accelerometer Sensor



Green CLK Circuitry

Modify from AMD review

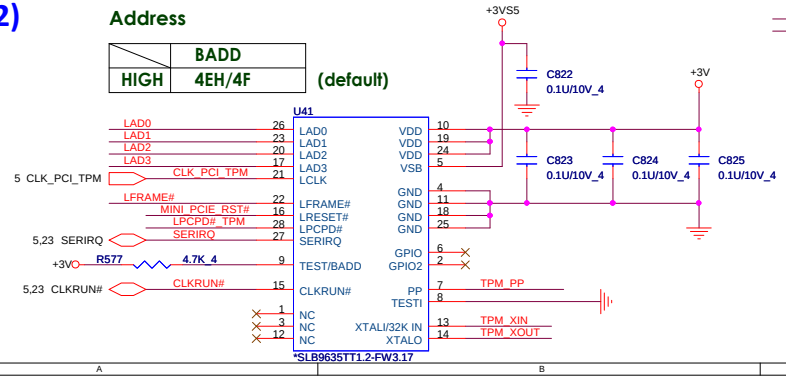


	U18 P/N
UMA	AL3NB242000
DIS	AL003357000

TPM (1.2)

Address

	BADD
HIGH	4EH/4F (default)



PROJECT :U93
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI-PCIE/LED	1A
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ITE pin 100 , 104 , 106 default can not pull up to +3VPCU it will cause chip into test mode

+3VPCU CAP close to EC pin

Smart adapter Type check

Change to 1SS355 as Current loss

D7 1SS355

DGPU Thermal protect

*ME2N7002E

For +VIN noise

Vender	Size	P/N
AIT	4M	AKE39ZN0800
GGD	4M	AKE39GN0Q01
WND	4M	AKE39FN0N01
Socket		DFHS08FS023

4M SPI EC ROM

A25LQ32AM-F/Q
AKE39GN0Q01
91960-0084L-8P-SOCKET

128K byte SPI EC ROM

ICT need TP2675 size test point

TP place on top lay for ICT request

*W25X40AVSSIG
DFHS08FS023
SOIC8-6-1_27

Adapter select

Hi ==> A6-5200 25W CPU + DIS
Low ==>UMA/DIS/SG

Platform model	GPIO42	adapter
A6 25W CPU + DIS	High	90W
DIS/SG/UMA	Low	65W

ADD VGA TEMP_ FAIL function is active Hi

PROJECT :U93
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EC (IT8528E)/ROM	1A

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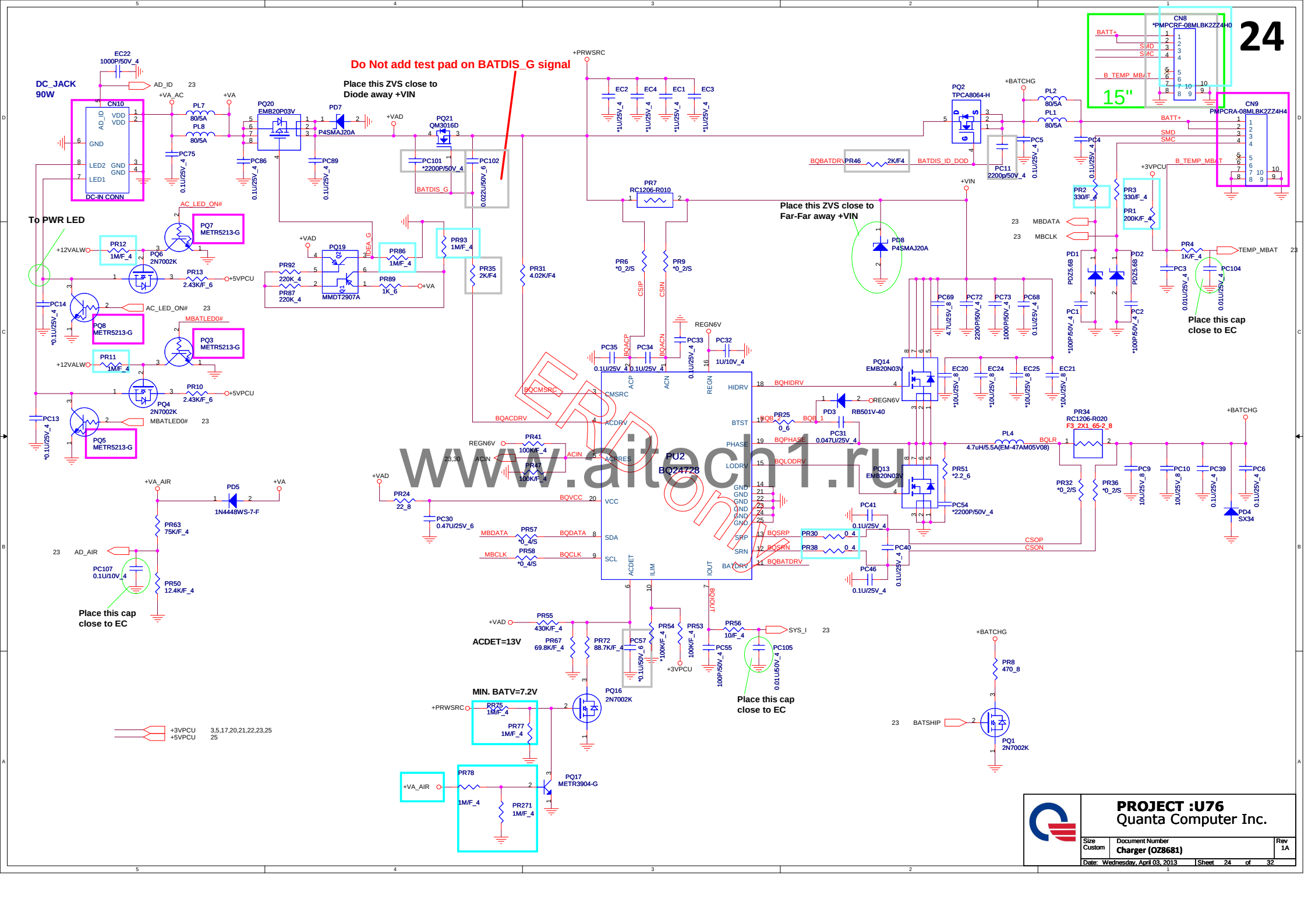
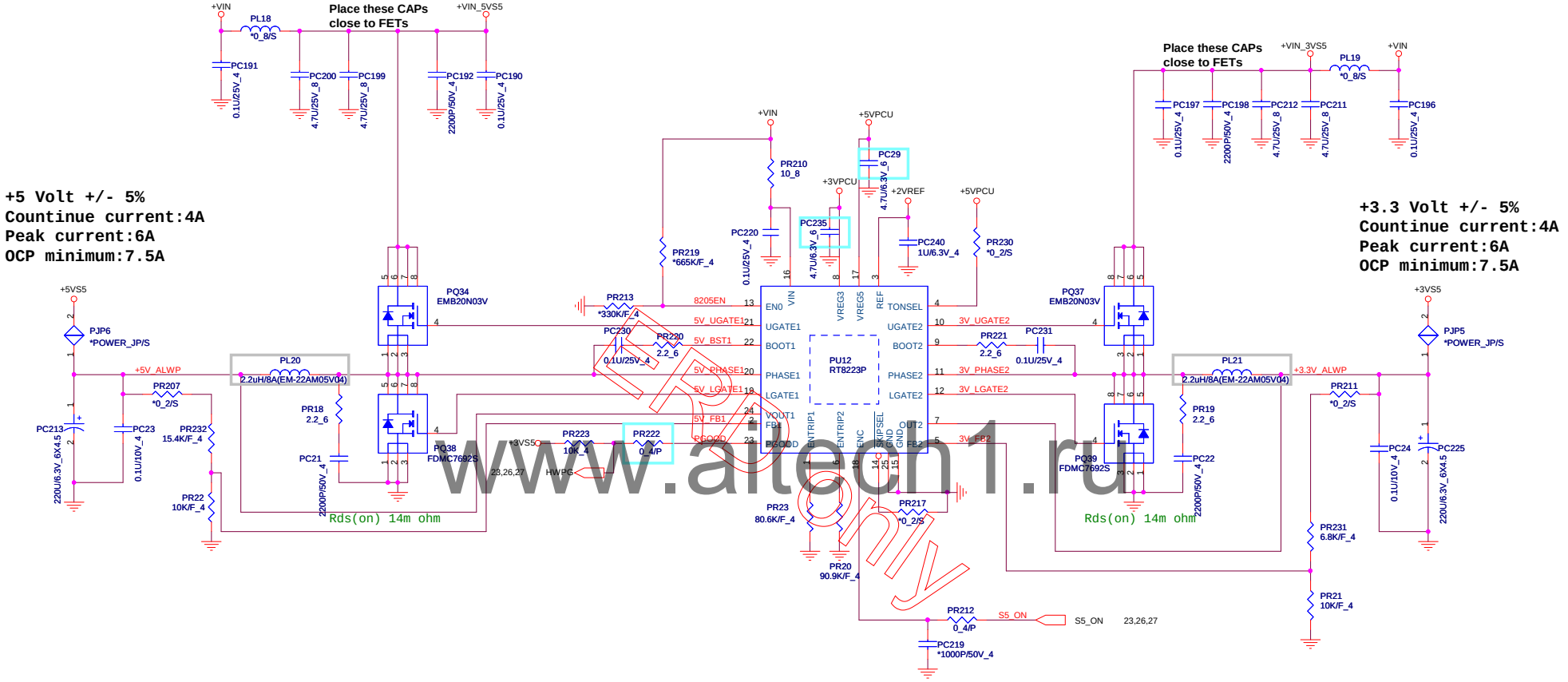
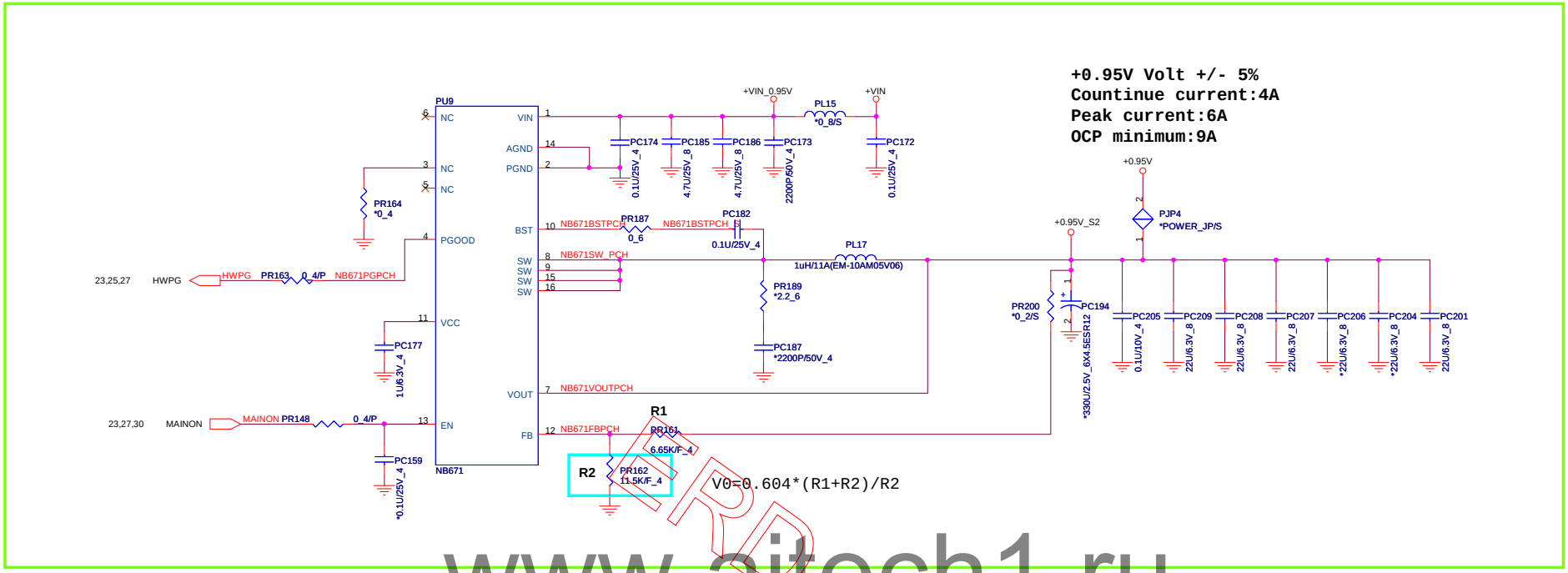

24
DC_JACK
90W
CN10
DC-IN CONN
Do Not add test pad on BATDIS_G signal
Place this ZVS close to
Diode away +VIN
To PWR LED
Place this ZVS close to
Far-Far away +VIN
Place this cap
close to EC
Place this cap
close to EC
Place this cap
close to EC
ACDET=13V
MIN. BATV=7.2V
BQ24728
PU2
CN8
*PMPCRF-08MLBK2ZZ4H0
15"
CN9
PMPCRA-08MLBK2ZZ4H4
www.aitech1.ru



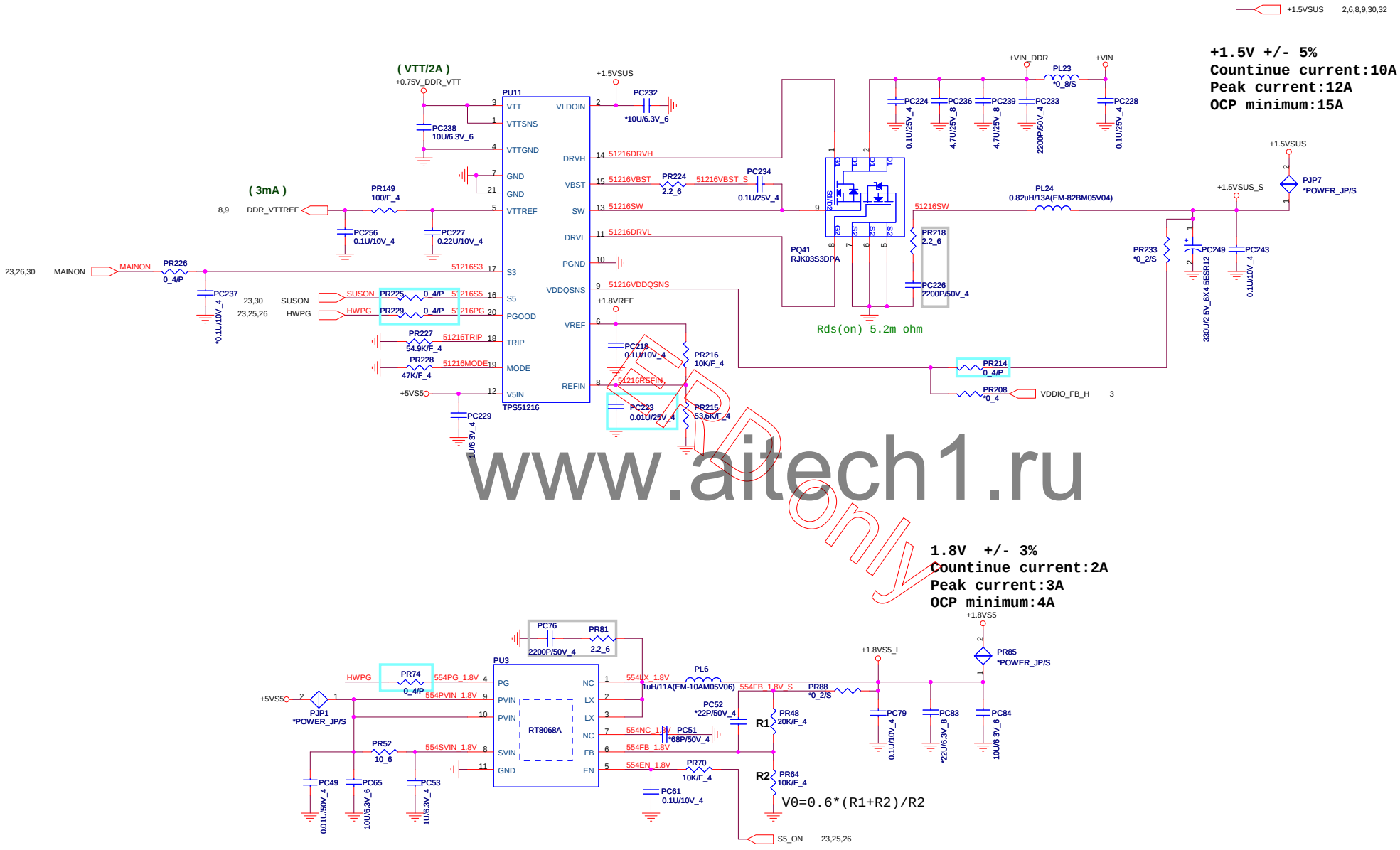
PROJECT :U76 Quanta Computer Inc.		
Size: Custom	Document Number: 3/5VPCU(RT8223P)	Rev: 1A
Date: Wednesday, April 03, 2013	Sheet 25 of 32	



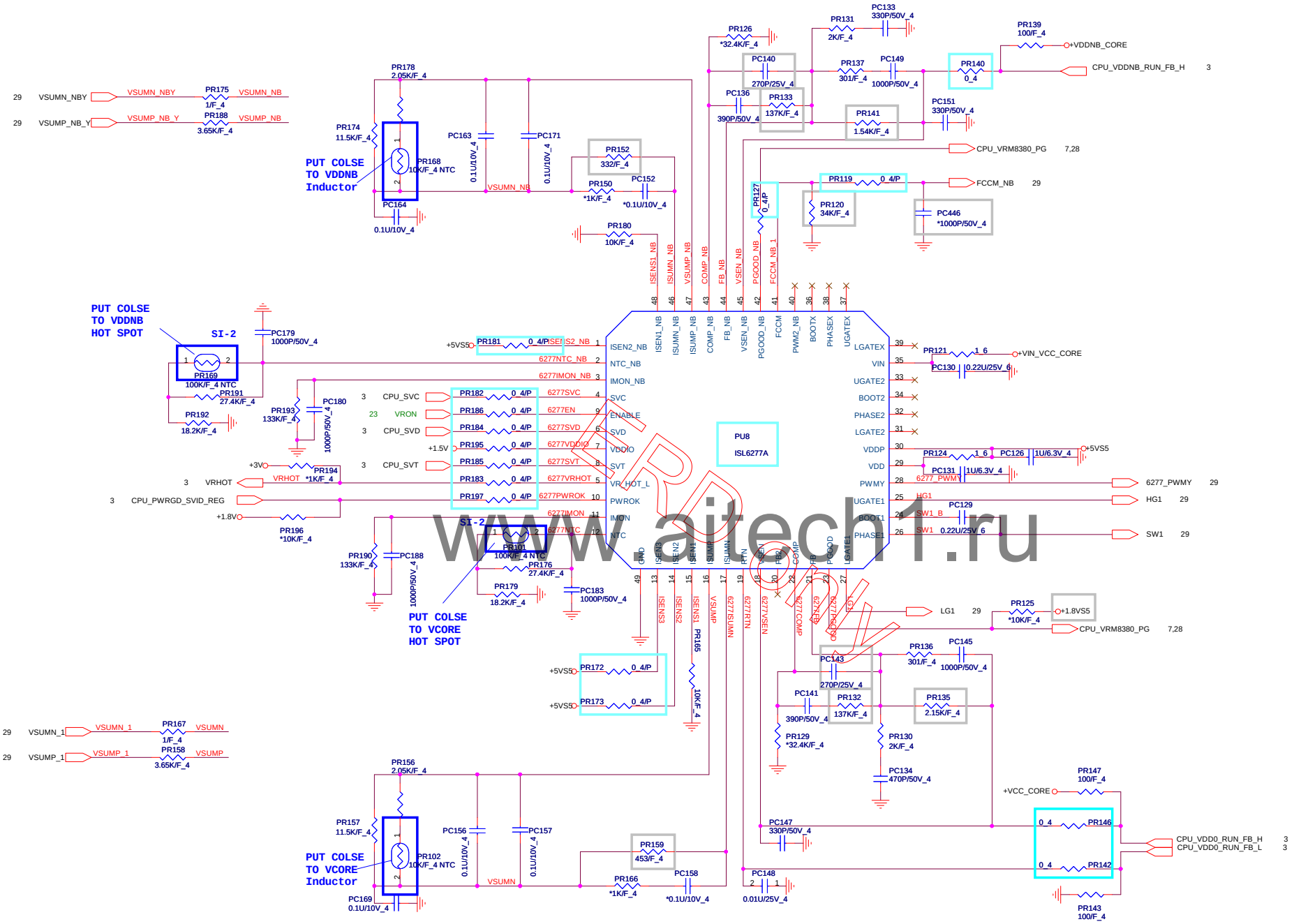
PROJECT :U76
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.2V (RT8228)	1A

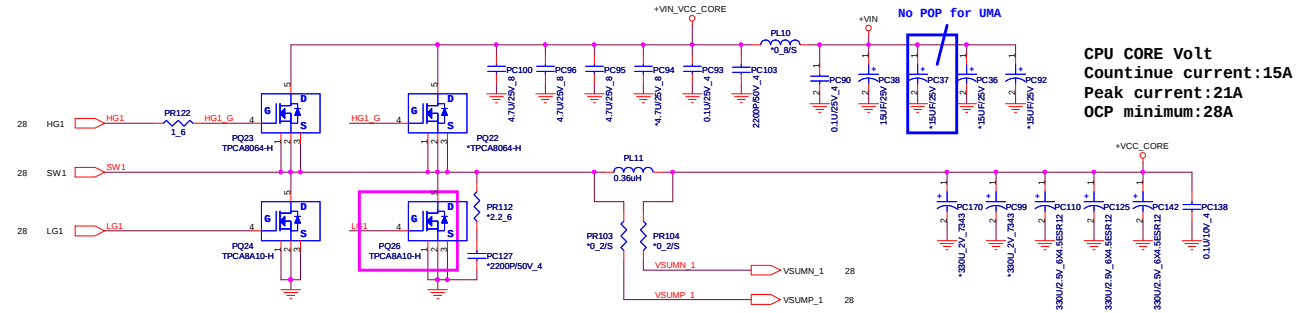
Date: Wednesday, April 03, 2013 Sheet 26 of 32



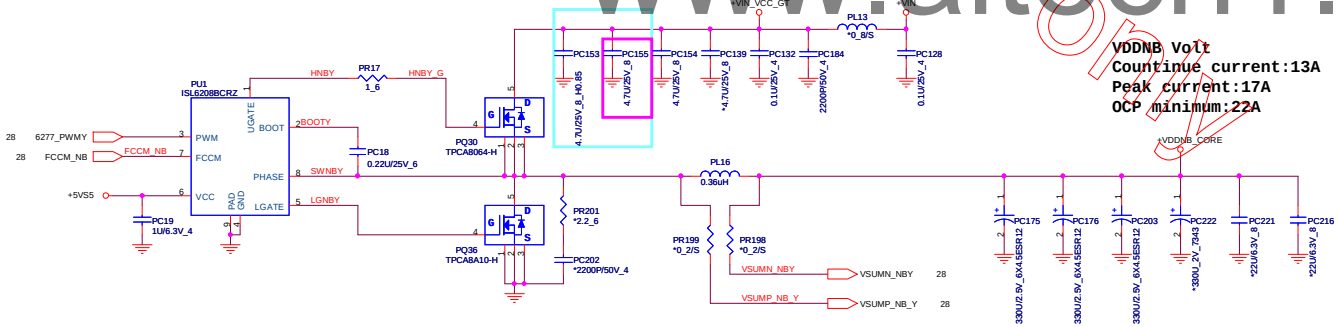
PROJECT :U76 Quanta Computer Inc.		
Size: Custom	Document Number: DDR3 (TPS51216)	Rev: 1A
Date: Wednesday, April 03, 2013	Sheet 27 of 32	



PROJECT :U76 Quanta Computer Inc.			
Size: Custom	Document Number: ISL6277		Rev: 1A
Date: Wednesday, April 03, 2013	Sheet 28 of 32		

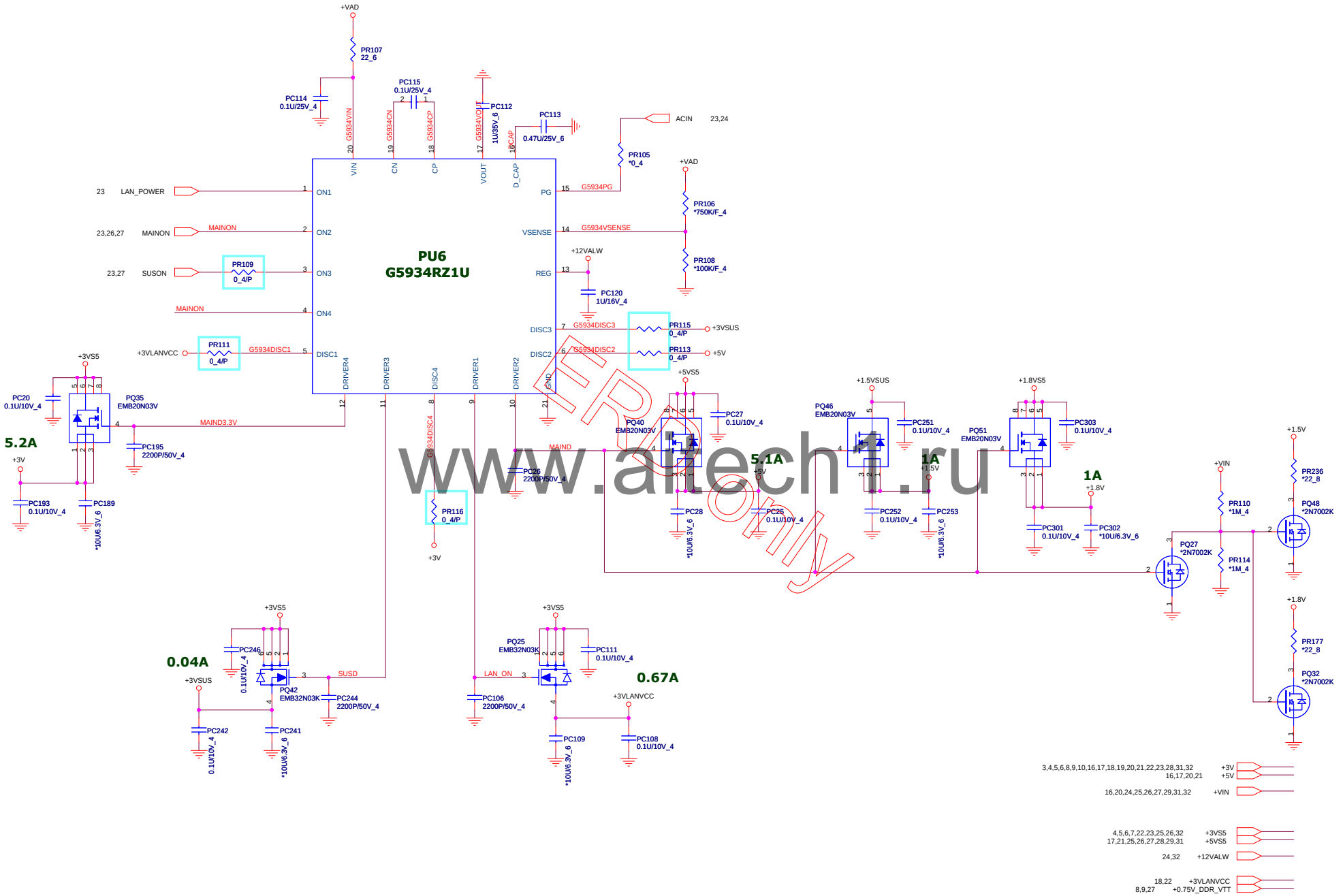


CPU CORE Volt
Countinue current:15A
Peak current:21A
OCP minimum:28A



VDDNB Volt
Countinue current:13A
Peak current:17A
OCP minimum:22A

PROJECT :U76 Quanta Computer Inc.			
Size: Custom	Document Number: ISL6208		Rev: 1A
Date: Wednesday, April 03, 2013	Sheet 29 of 32		



PROJECT :U76
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Dis-charge IC (SLG55448V)	1A

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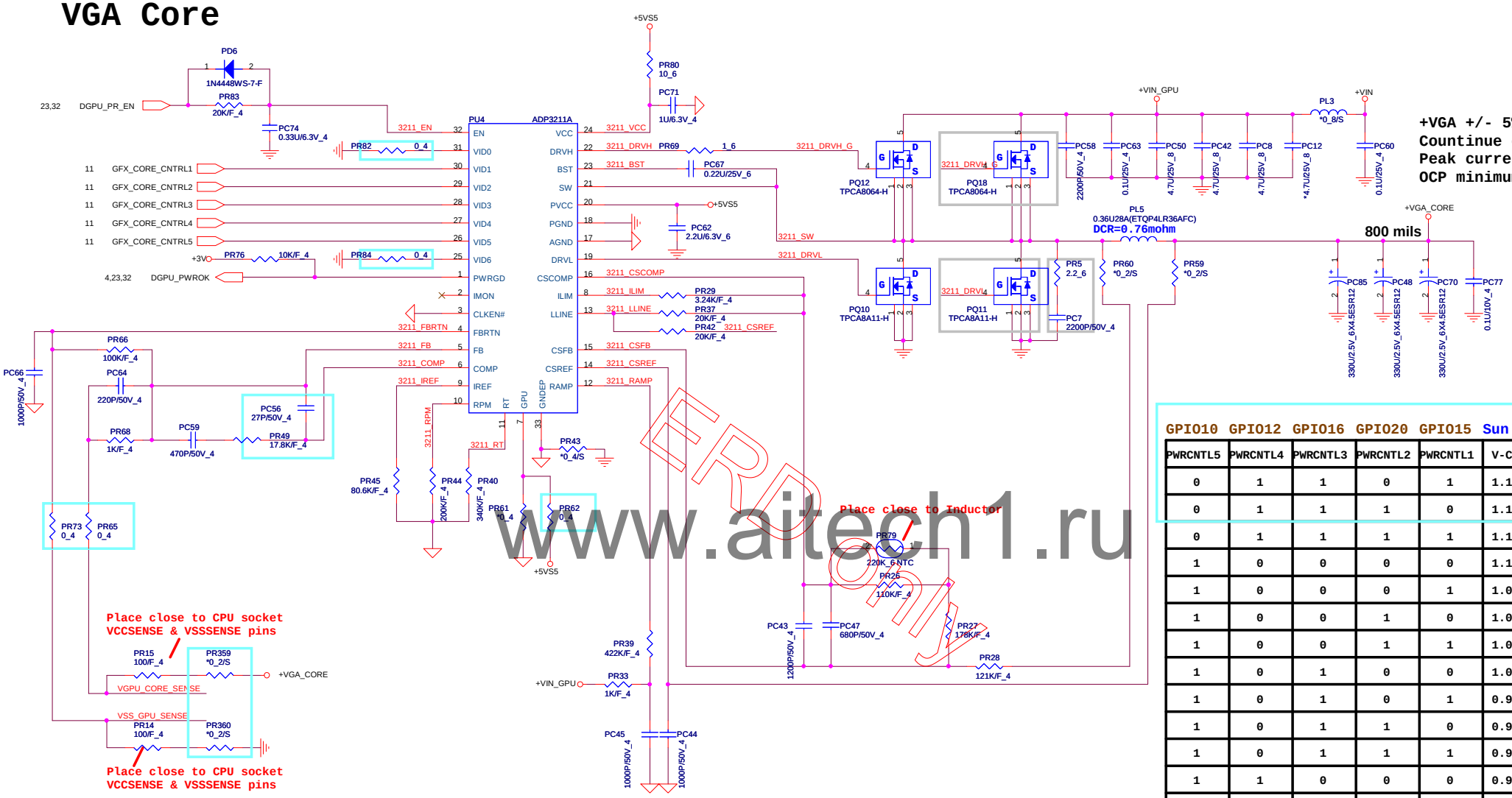
VGA Core



+VGA +/- 5%
Countinue current:21A
Peak current:27A
OCP minimum 33A

GPIO10 GPIO12 GPIO16 GPIO20 GPIO15 Sun S3

PWRCNTL5	PWRCNTL4	PWRCNTL3	PWRCNTL2	PWRCNTL1	V-CORE
0	1	1	0	1	1.175V
0	1	1	1	0	1.150V
0	1	1	1	1	1.125V
1	0	0	0	0	1.100V
1	0	0	0	1	1.075V
1	0	0	1	0	1.050V
1	0	0	1	1	1.025V
1	0	1	0	0	1.000V
1	0	1	0	1	0.975V
1	0	1	1	0	0.950V
1	0	1	1	1	0.925V
1	1	0	0	0	0.900V
1	1	0	0	1	0.875V
1	1	0	1	0	0.850V
1	1	0	1	1	0.825V
1	1	1	0	0	0.800V
1	1	1	0	1	0.775V

Default

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE NCP3218G)	1A

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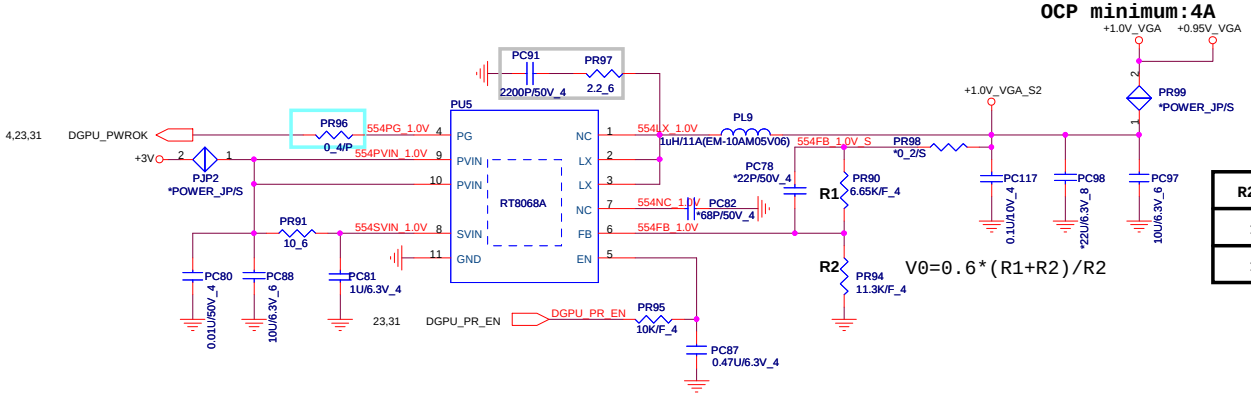
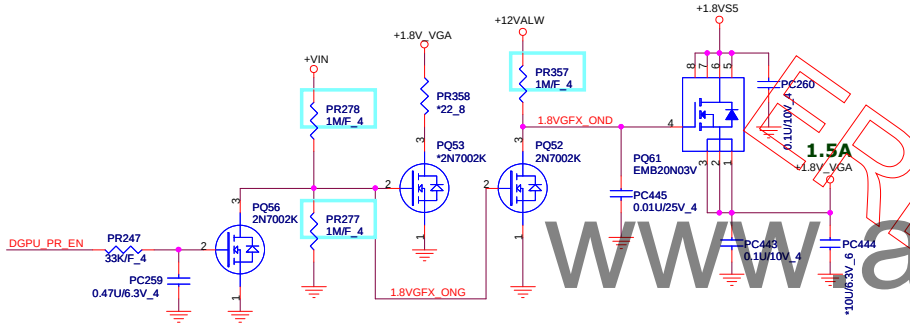
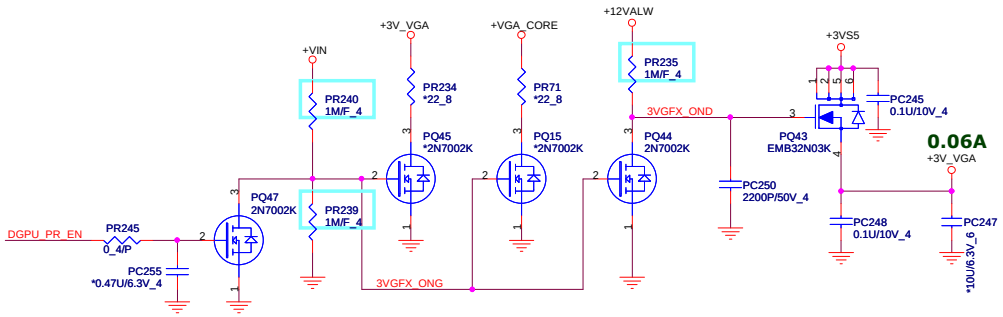
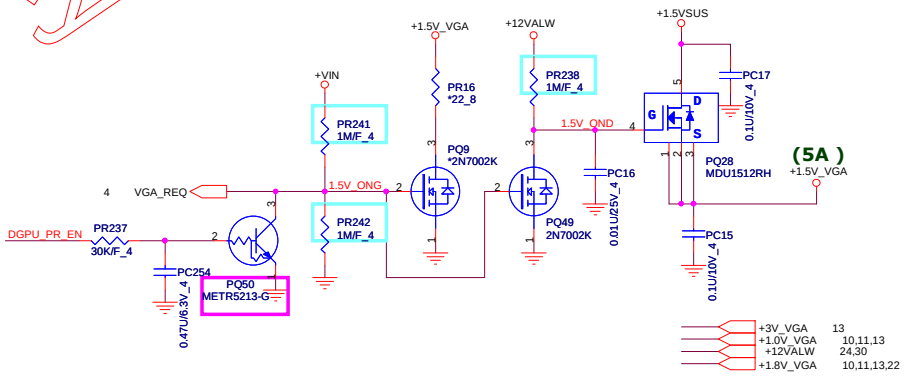
+0.95V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A



R2 Value	P/N	1.0V_VGA
10K	CS31002FB26	1.0V
11.3K	CS31132FB07	0.95V







PROJECT :U76
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGA POWER	1A
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